



A HISTORICAL ANALYSIS OF FIBER BASED OPTICAL BUS PARALLEL COMPUTING MODELS

BRIAN J. D'AURIOL* AND MARIA BELTRAN†

Abstract. A comprehensive overview and survey of the developments in optical bus parallel computing models is presented in this paper. The first model proposed was the APPB in 1990. Since then, in the order of their appearance, the remaining nine models surveyed are: APPBS, ASOS, LPB, RASOB, AROB, LARPBS, PB, LAPOB and PR-MESH. Research trends observed from this analysis indicate periods of model development leading to more and more sophistication and complexity in the model, followed by periods of model simplifications. These periods appears to occur in cycles. We note the widespread and global research interest in these models. The three most popular models appear to be RASOB, AROB and LARPBS. We also have analyzed a crucial aspect of these models, the bus cycle time definitions, and have determined inaccuracies in most of the definitions appearing in the literature. We also provide refinement to the definitions to correct such inaccuracies.

Key words. Optical Bus, Parallel Computing

1. Introduction. Optical fiber bus interconnection parallel computing models were initially proposed over a decade ago. Since then, at least ten distinct models have been developed with many corresponding publications. In addition, related work on implementation as well as routing and addressing have been noted. A principal reason for the success of this research area stems from the advantages of optical communications together with bus-based systems. Some of the advantages include inherent pipelining of messages due to the unidirectional propagation nature of optical signals as well as power speed and crosstalk advantages over electronic buses [1].

A comprehensive overview and survey of the developments in optical bus parallel computing models is presented in this paper. This survey includes ten optical bus models that were proposed between the period of 1990 to 2000. Many publications have appeared and publications continue to be submitted based on these models. First, a description of the salient parts of optical buses is given. Next, the ten surveyed models are described. Observations regarding similarities and differences inherent in the models are noted. Lastly, some analytical comments are presented.

Several papers provide survey-type information. These survey papers [2, 1] are not reported in the model summary sections. This paper actually extends the work of the above survey papers.

The purposes of this paper are three-fold. First, to provide to the computer professionals who do not have detailed knowledge of optical bus parallel models an introduction and overview of the major points of these models as well as providing information about the various proposed models. Second, to provide to the research community a handy-reference of first citations, categorizations of existing publications and a source of additional material to consider. Third, to provide to the research community an extensive literature bibliography.

The paper is organized as follows. A review of basic concepts in optical bus parallel models is given in Section 2. In Section 3, a brief overview of ten optical bus models with an emphasis on bus cycle is given. Historical comments are made in Section 4. An analysis of bus cycles definitions in these models is given in Section 5. Conclusions are given in Section 6

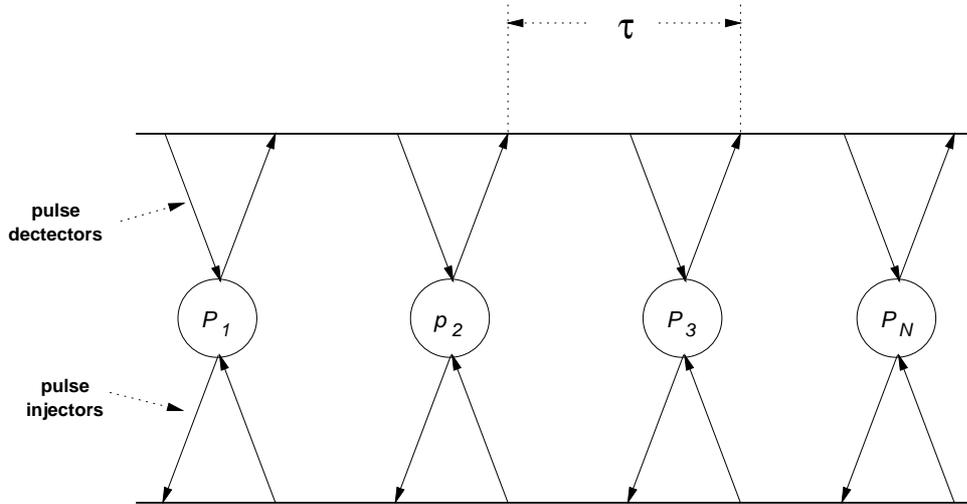
2. Optical Bus Model. In general, an optical bus model uses one or more optical waveguides to connect a linear array of N processors labeled 0 through $N - 1$. This architecture can be extended to more than one dimension where, for example, processors are arranged in a matrix. Processors are connected to the waveguides by injectors, which inject light pulses onto the waveguide(s), and detectors, which detect light pulses on the waveguide(s). The time it takes a pulse to traverse the distance between any two adjacent injection points (or two detection points) is a constant commonly referred to as τ , while the duration of the pulse is usually referred to as ω . In the literature, one simple case of collision is addressed by defining b as the maximum size of a message such that $b\omega < \tau$.

There are four aspects of optical bus models that may be used as criteria for classification: (1) the number of buses to which processors are connected, (2) the type of bus that is used (folded or non-folded), (3) the dimension of the model, and (4) the type of addressing used. These aspects are detailed below.

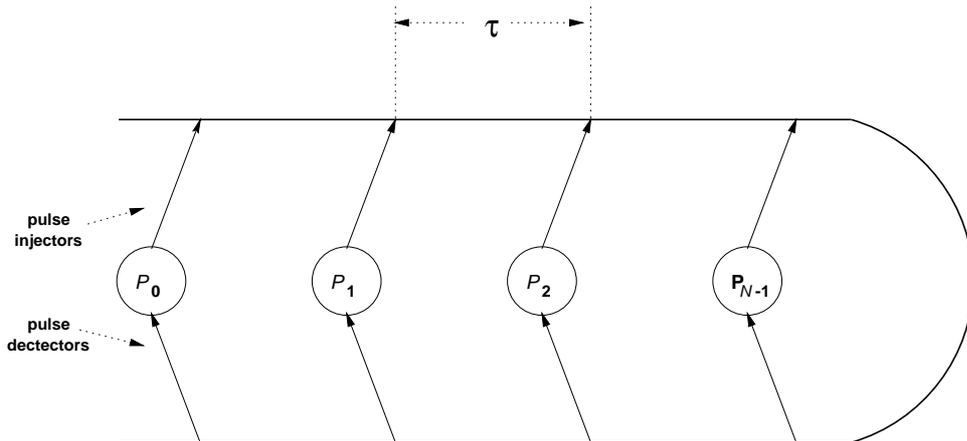
In order to enable all processors arranged in a linear array to communicate with each other, the interconnection network must allow traffic to travel in two directions. Due to the unidirectional propagation property

* (dauriol@acm.org).

†CAS Inc., El Paso, TX, USA (maria.beltran@cas-west.com).

FIG. 2.1. *Non-folded (Two) Bus Configuration*

of light, however, a single optical bus running along the length of the array will only allow communication in one direction. The directional requirement is fulfilled by using two buses. Figure 2.1 illustrates this. Note that processors are connected to both buses by both injectors and detectors. The two buses in this configuration are referred to as non-folded buses. The folded bus, on the other hand, combines both directional requirements into a single bus. It is a single bus that parallels the array of processors, and is folded around one of the ends of the array. This enables light to travel in both directions with respect to the processors. Typically, the linear segment before the fold is called the transmitting segment while that after the fold is called the receiving segment. On the transmitting segment, processors are connected by injectors and on the receiving segment, by detectors. The time it takes a pulse to traverse the fold of the bus is a constant that is denoted as γ , and is not necessarily a multiple of either τ or ω . Figure 2.2 shows the folded bus architecture.

FIG. 2.2. *Folded (Single) Bus Configuration*

This description of the optical bus architecture applies to one-dimensional (or 1-D) models. This architecture is used as a building block for models consisting of more than one dimension. The most common multi-dimensional model found in the literature is the two-dimensional (or 2-D) model. In such a model, processors are arranged in a matrix format and the optical buses belong to one of two groups, rows or columns. The orientation of the row buses is perpendicular to that of the column buses. The two-dimensional model has been found to be helpful in reducing time delays in message delivery. Depending on the model, there are various ways that row and column buses can be connected to each other and to the processors. Reconfigurable switches

are commonly used to make connections at intersection points. Examples of the use of reconfigurable switches can be found in [3, 4, 5, 6, 7].

The literature search indicates that, in models that use more than one waveguide, models with three waveguides are the most commonly used configuration. Coincident pulse addressing, discussed subsequently, is the primary reason why three waveguides are used. Most of the models that employ more than one waveguide provide one for the message and the remaining two for addressing purposes. The two addressing waveguides it uses are referred to as the select and reference waveguides.

Coincident pulse (CP) is the most common form of addressing. Delays of duration ω are placed between every pair of detectors on the reference and message waveguides to implement CP. Addressing works as follows: first, the source processor sends a pulse on the reference waveguide at the same time it starts to send the message on the message waveguide. Then the processor waits a factor of ω , depending on the destination processor it wishes to communicate with, to send a pulse on the select waveguide. The pulse on the reference waveguide is delayed by the delays on the receiving segment such that it will be detected by the intended destination processor at the same time as the select pulse. At that point the message, which also arrives at the intended processor at the same time as the select and reference pulses, is read in from the message waveguide. Figure 2.3 shows a folded bus with the coincident pulse addressing components.

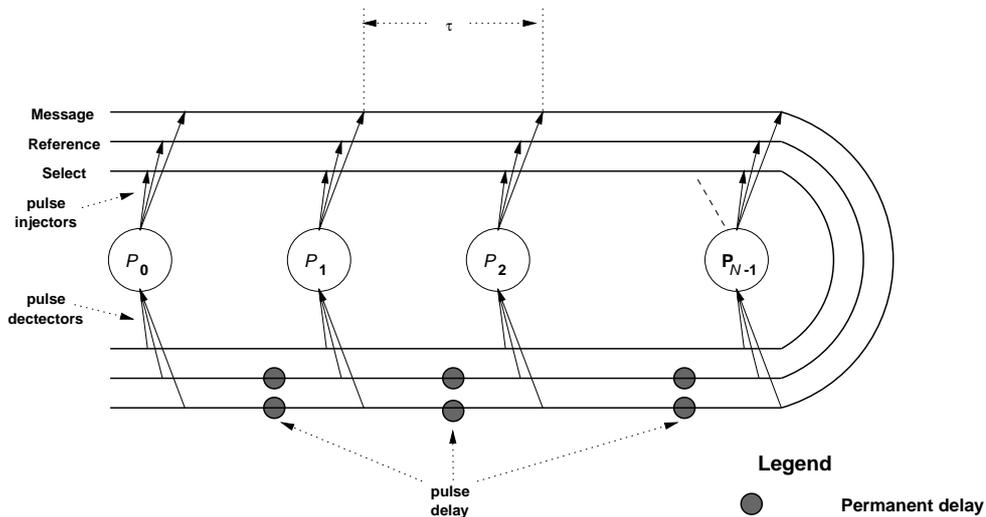


FIG. 2.3. *Folded Bus with Coincident Pulse*

The other commonly used addressing method is time-division multiplexing (TDM). This method involves assigning a particular time slot for a particular processor. This time slot can either be used to send (time-division source multiplexing, or TDSM) or receive (time-division destination multiplexing, or TDDM) optical signals. More detail regarding these bus aspects can be found in [2, 1, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17].

The next section briefly describes the various bus models found in the literature. A point of interest in each section is the information regarding the use of the term ‘bus cycle’. A subsequent section critiques the overall use of this term.

3. Optical Buses in the Literature. This section surveys ten optical bus models found in the literature. The first one was proposed in 1990 while the last in 1998. Figure 3.1 depicts the optical bus model development in a timeline.

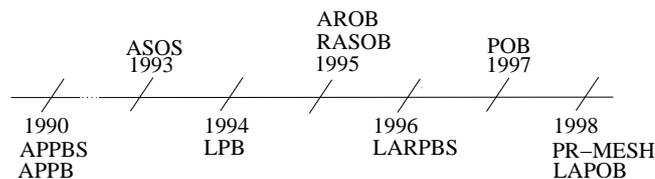


FIG. 3.1. *Optical Bus Model Timeline*

3.1. APPB (1990). The first proposed optical bus model is the Array of Processors with Pipelined Buses (APPB) [3], which can be one or two dimensions. In one dimension, there are two optical buses that are placed parallel to and on either side of a linear array of N processors. Each processor is connected to each bus via one injector and one detector. This allows a processor to communicate with any other processor. The bus cycle time is $N\tau$ time units. In two dimensions, each processor is connected to four buses by a switch, two row buses and two column buses. For this configuration, a bus cycle is defined as $N_1\tau$ for a row bus and $N_2\tau$ for a column bus. In addition, the authors define a *petit bus cycle* as τ . APPB uses either TDM or CP for addressing and routing. For the TDM method in the one dimensional configuration, a set of two control functions, *send* and *wait*, are used to control access to the optical bus. The two dimensional APPB adapts the *send* and *wait* and introduces the *relay* function to provide control of messages between different rows (messages travel row-wise first). Figure 3.2 illustrates the one dimension architecture, while Figure 3.3 illustrates the two-dimensional architecture. Individual waveguides are not shown. Rather, the optical bus is represented by a single line. Variations of APPB that incorporate folded bus and conditional delay switches are discussed in [18]. Papers reporting work on APPB are [3, 19, 20, 21, 22, 23, 24, 25, 26, 27].

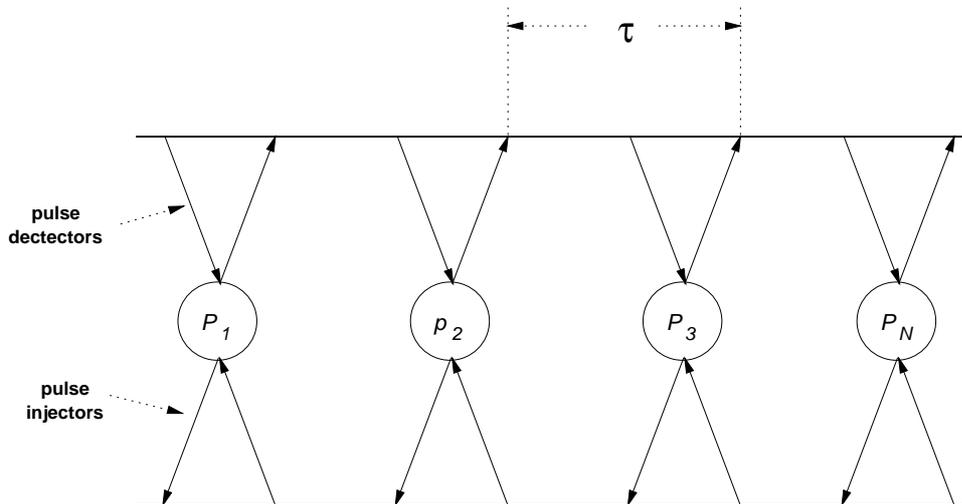


FIG. 3.2. APPB 1-D Architecture

3.2. APPBS (1990). The Array of Processors with Pipelined Buses Using Switches (APPBS) [3] is the same as the 2-D APPB; with one important difference. In this model, switches are used at every intersection of row and column buses, thus, eliminating the need for processors to act as relays between the buses. As with the APPB, APPBS can use TDM or CP addressing methods and the bus cycle is $(N_1 + N_2)\tau$. Switch configurations impact the communication. Each of the switches can be configured as straight or crossed and can be dynamically reconfigured relative to the start of the bus cycle (by using petit cycles). This flexibility requires additional conditions to ensure collision-free communication, especially when messages need to be switched at the same place and time. Algorithms such as matrix transpose, binary tree routing, and perfect shuffle are implemented in a one step operation. This one step not only includes bus cycle time but also the time to process some messages and the switch setup time. Figure 3.4 illustrates this model. Individual waveguides are not shown. Papers reporting on APPBS are [3, 20, 23, 24, 28, 29].

3.3. ASOS (1993). The Array Structure with Synchronous Optical Switches (ASOS) [4] is a two-dimensional model that uses multiple folded buses. This type of architecture consists of a single waveguide folded around a linear array of N processors. A 2×2 switch is placed at the intersections of receiving segments of row buses and transmitting segments of column buses. Each processor is connected to the transmitting and receiving segments of the row bus, but only connected to the receiving segment of the column bus. ASOS uses a combination of TDSM and TDDM to route messages between rows and columns; and the CP method for destination addressing. The term bus cycle is not explicitly mentioned, however, the end-to-end propagation delay of a row bus is mentioned and is defined as $(2N - 1)D$ (where D roughly corresponds with the τ elsewhere). This equation includes the delay for the fold, which is set to D . One additional architectural feature is due

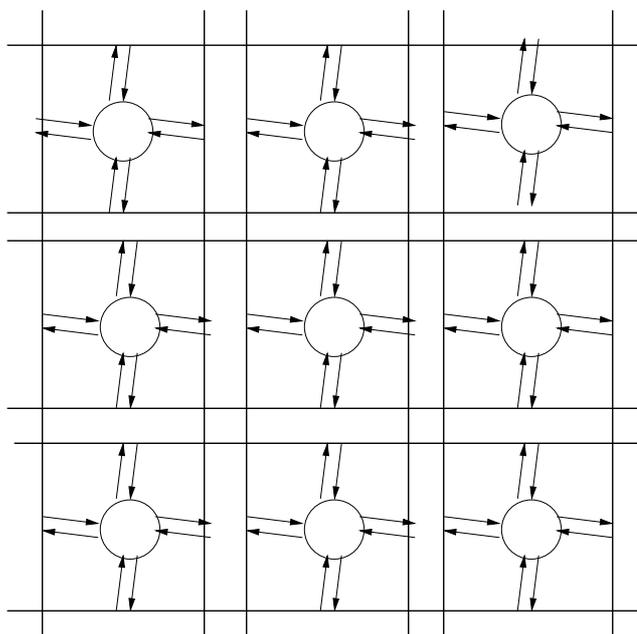
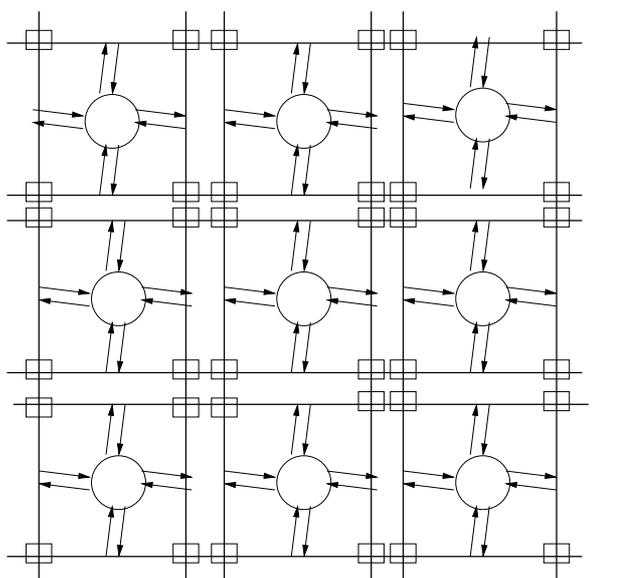


FIG. 3.3. APPB 2-D Architecture



Legend
 □ Switch

FIG. 3.4. APPBS Architecture

to the bus contention that occurs if more than one processor sends a message to the same column bus. To alleviate this, a *reservation* waveguide is included in each row bus. Processors needing to send messages use this waveguide to determine if there already is a message that would contend with theirs. Priority schemes are used to establish conflict resolution. Figure 3.5 illustrates this architecture. Individual waveguides are not shown. A modified architecture called the Symmetric ASOS (SASOS) is presented in [30]. We point out that the authors in [6] refer to this model as ASOB; more likely, the authors appear to refer to the RASOB model (see below).

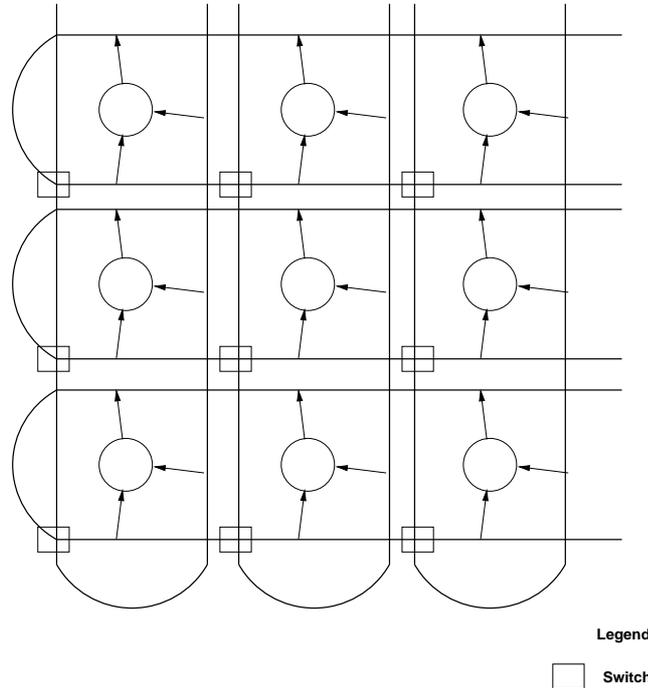


FIG. 3.5. ASOS Architecture

3.4. LPB (1994). The Linear Pipelined Bus (LPB) model appears in 1994 in [8]. There is some contradicting evidence in the literature pertaining to the definition and origin of the LPB model. The authors of [28] cite [31], which has similar title, as a source for this optical bus model. However, upon a review of that paper, it is concluded that the content does not include optical buses. It is possible that the authors inadvertently cited the 1995 paper instead of the 1994 paper. The author of [32] cites reference #59, a submitted paper as the source for LPB, yet that paper was not published as cited. It is possible that, in reality, that submitted paper is [33] (which has a different title but the same authors, albeit, in a different order). Personal communication with the author of [32] confirms that the submitted paper was indeed published but under a different title and different author order. In [33], the authors cite the 1994 paper as the source of LPB. Hence, it is concluded that the 1994 publication [8] is the original source of LPB.

LPB is a one-dimensional model that uses the folded bus. It not only has the fixed delays on the receiving segments of the reference and message waveguides, but also has conditional delays between every pair of injection points on the select waveguide. A bus cycle is defined as the end-to-end propagation delay on the bus and is presented prior to including the use of conditional delays (which make the end-to-end propagation delay a variable). The bus cycle formula is defined as $2N\tau + (N-1)\omega$. Figure 3.6 illustrates this architecture. Individual waveguides are shown, including the placement of delays. S_1, \dots, S_{N-1} denote the conditional delays, each controlled by processors P_1, \dots, P_{N-1} , respectively. We note the similarity with the LARPBS model described later; in comparison, this model is not reconfigurable and uses a slightly different addressing technique. Papers reporting on LPB are [8, 34, 33, 31].

3.5. RASOB (1995). The Reconfigurable Array with Spanning (or Slotted) Optical Buses (RASOB) [5] is similar to ASOS. The architecture was initially designed to support SIMD processing and to contain less complexities than ASOS. It uses the folded bus, and can be one or two dimensional. In the former, each processor is connected to the bus on the transmitting and receiving sides. In the latter, there is an $N \times N$ matrix of folded buses. As in ASOS, one 2×2 switch is placed at each intersection of row and column buses. Each processor is connected to the buses: two connections for receiving (one for row, one for column) and one for transmitting. A constraint that no more than one processor per row can send a message to processors in the same column exists in a communication cycle. Either a TDDM or TDSM method is used for addressing. The authors state that support for MIMD processing could be accomplished by using coincident pulses, however, doing so would make the architecture more complex. The bus cycle for RASOB is defined as $4N\tau$ where a row

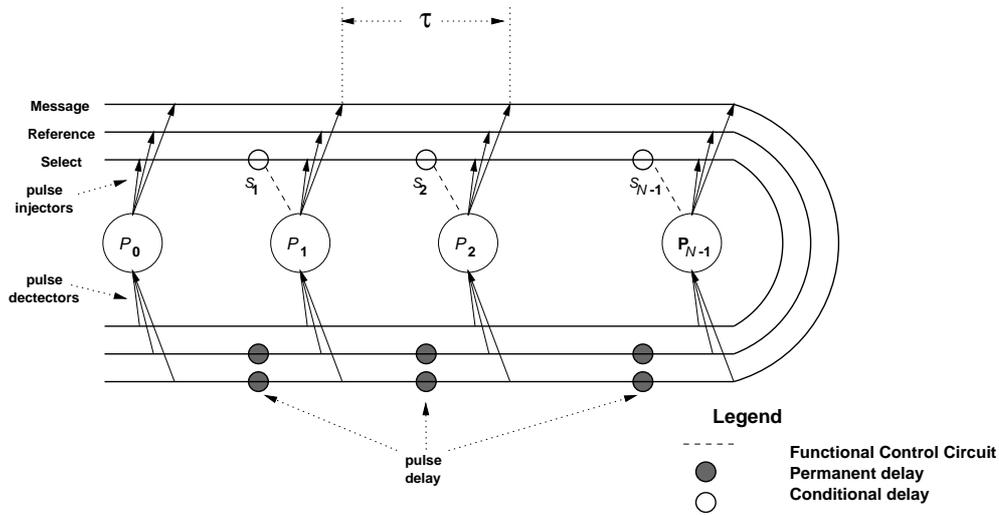


FIG. 3.6. LPB Architecture

bus has $2N\tau$ cycle time. Figure 3.7 illustrates this architecture. The figure shows a 3×3 RASOB. Individual waveguides are not shown. Papers that report on RASOB are [5, 35, 36, 37, 38, 39, 40, 41, 42, 43].

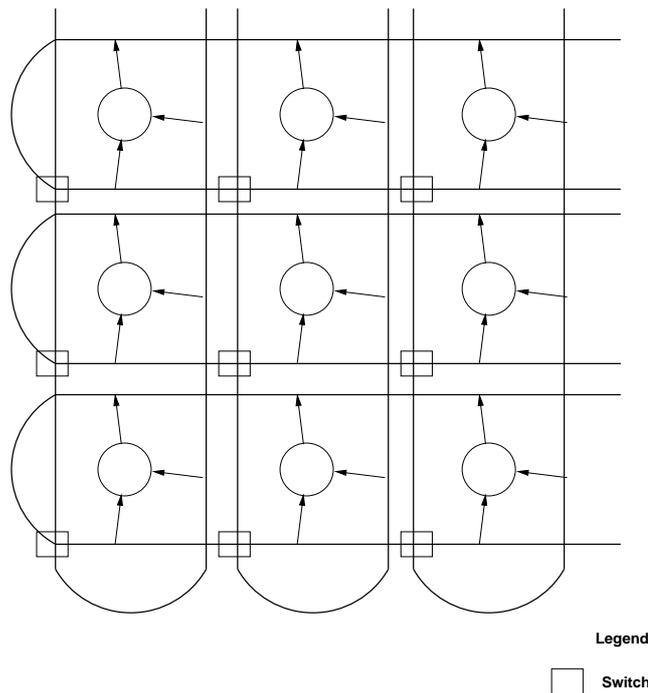


FIG. 3.7. RASOB Architecture

3.6. AROB (1995). The Array with Reconfigurable Optical Buses (AROB) [6] also uses the folded bus. The AROB is an $N_1 \times N_2$ reconfigurable mesh where each processor contains registers for the temporary storage of messages being routed. Processors use an internal switching system to reconfigure the network by connecting or disconnecting four I/O ports to each other. Two of the ports are connected to either segment of the row bus while the other two ports are connected to the column bus. Both TDM and CP can be used for addressing. Notable is that communication involves *counting* by processors. Thus, the communication time must also incorporate some processing time overhead. Since the processing time can be orders of magnitude

greater than the end-to-end propagation time, the processing time order must be of the same magnitude as that of the end-to-end propagation time: this is achieved by the condition that the number of processors must be greater than the ratio of the processing time to communication time (subject to an appropriate bus length). Two other features of the AROB are its bit polling capability and its capability to introduce/adjust signals by multiple unit delays per processor [28, 33]. Bit polling is the ability to select the k^{th} bit of a group of messages and determine the number of one bits. Figure 3.8 illustrates this architecture. The figure shows a 3×3 AROB. Individual waveguides are not shown. Papers that report work on AROB are [6, 25, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 29, 28, 61, 62].

A $1 \times N$ (one-dimensional) AROB is commonly referred to as a Linear AROB or LAROB. The bus cycle time for LAROB is defined slightly differently in different papers. In [6] it is defined to be the end-to-end propagation delay: $2N\tau$ plus some processing time. In [57], it is defined slightly differently, to be only the end-to-end propagation delay: $2N\tau$. Each processor controls its pair of bus connection switches. When these switches are set crossed at a processor, the bus is split into two at that point. In [60], AROB is extended to multi-dimensions.

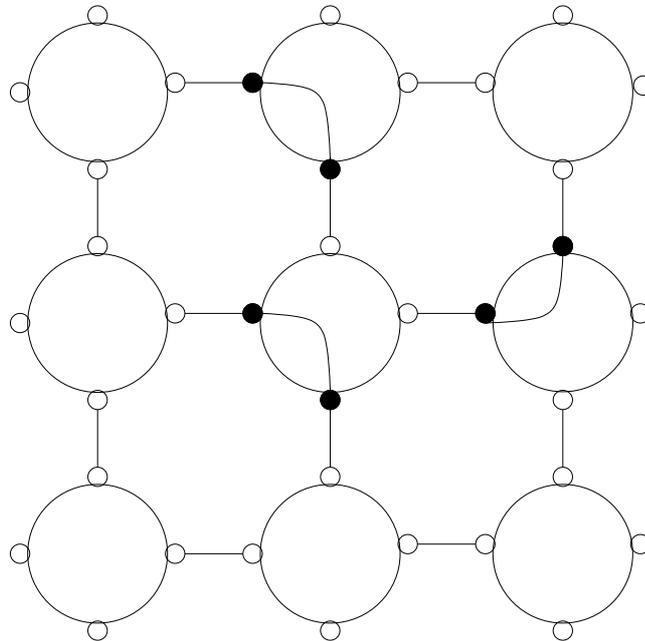


FIG. 3.8. AROB Architecture

3.7. LARPBS (1996). The Linear Array with a Reconfigurable Pipelined Bus System (LARPBS) [63] is a one dimensional reconfigurable folded bus model. It contains $N - 1$ fixed delays on the receiving side of the reference and message waveguides and $N - 1$ conditional delays on the transmitting side of the select waveguide. Switches allow partitioning of the bus. Addressing can be done by either TDM or CP. The bus cycle is the end-to-end propagation delay on the bus: $2N\tau + (N - 1)\omega$. Unlike AROB, LARPBS does not allow counting by processors. However, at the beginning of a bus cycle, each processor must set the conditional switches. Due to this (and other factors), the authors claim that LARPBS, unlike theoretical models such as PRAM, can be practically implemented by current (as of 1996) optical technology. Refer to [64] for a current discussion on implementation technology. Figure 3.9 illustrates this architecture. Individual waveguides are shown, including the placement of delays. $S_1 \dots S_{N-1}$ denote the conditional delays, each controlled by processors P_1, \dots, P_{N-1} , respectively. B_i^t and B_i^r , $0 \leq i \leq N - 2$, denote the pair of switches controlled by P_i which partition the bus. Papers reporting on LARPBS are [63, 65, 9, 66, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 32, 78, 79, 80, 81, 82, 34, 83, 33, 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95, 96, 97, 64, 98, 99, 100, 101, 102, 103, 104].

3.8. POB (1997). The Pipelined Optical Bus (POB) [10] model is a one-dimensional folded bus model. It contains N conditional delays on the receiving side of the reference waveguide that are controlled by processors

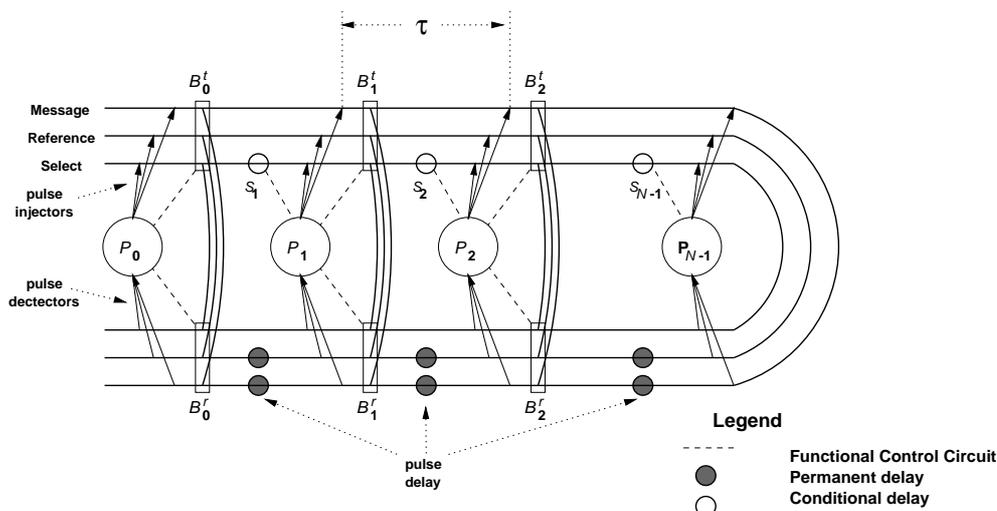


FIG. 3.9. LARPBS Architecture

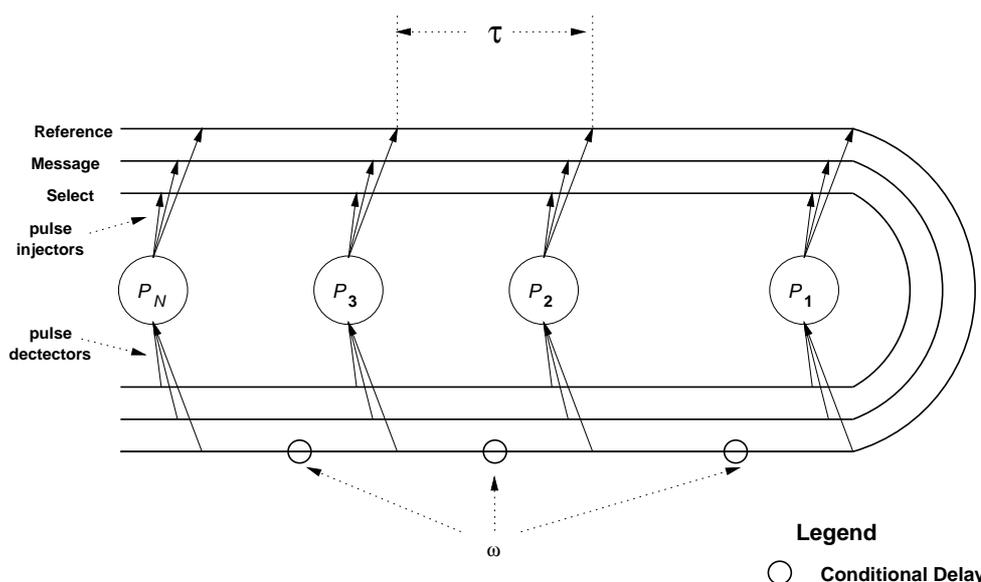


FIG. 3.10. POB Architecture

as needed. Addressing is done with either TDSM or CP. There is a possible problem that may occur when a message and a coincident pulse arrive at a destination processor at the same time: during the detection time interval for a coincidence pulse, part of the message could have already passed by. The *offset message transmission scheme* (OMTS) addresses this problem by sending the message a little after the select pulse (the end of the previous message stream is allowed to overlap with the next set of addressing pulses). The bus cycle time is the time that it would take N consecutive packet slots to propagate along the bus. The length of a packet slot is measured in time units, i. e., the larger of the length of the message or the total length of its associated sequence of select pulses: at most $D = \tau$ units. The model is described by the authors as “more powerful” than APPB and “more cost-effective” than LARPBS. Figure 3.10 illustrates this architecture. Individual waveguides are shown, including the placement of delays. Papers that report on POB are [10, 105, 15, 34, 33]

3.9. LAPOB (1998). The Linear Array of Pipelined Optical Buses (LAPOB) [11] is a one-dimensional folded bus model. It uses the CP addressing technique. Besides the fixed delays on the receiving segment, there are no other delays or switches on the bus. Each processor can only send one message in a single bus cycle. However, each processor contains special electronic hardware that allows it to address multiple processors if the

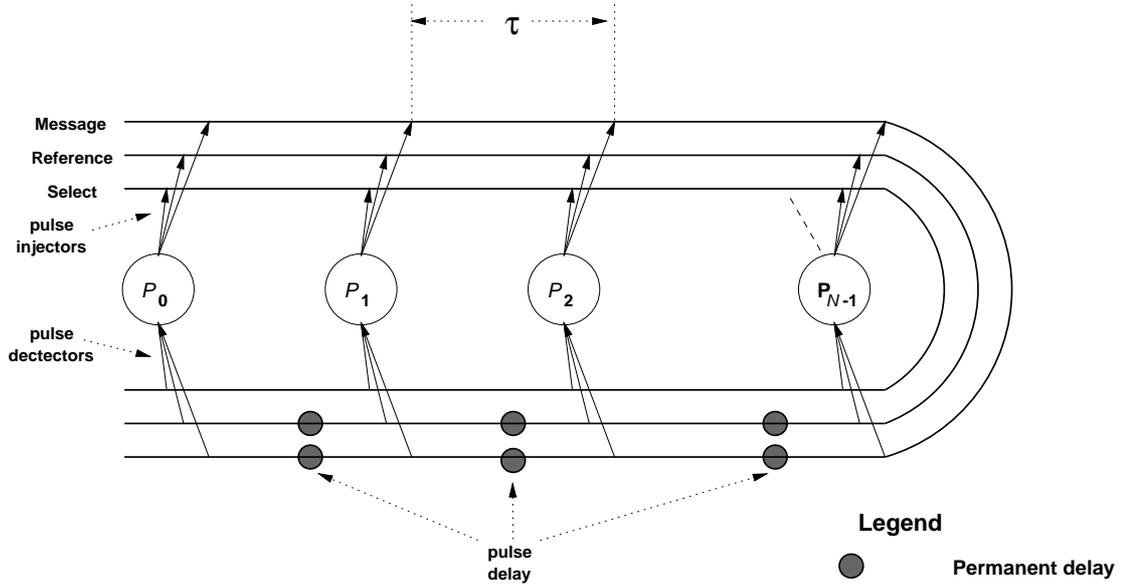


FIG. 3.11. LAPOB Architecture

positions of the destination processors form one of two patterns: contiguous interval (a sequence of adjacent processors) or regularly spaced. The formula for a bus cycle is not given in the paper. One advantage is that reconfiguration hardware is unneeded and, because of this, the model is less complex. Figure 3.11 illustrates this architecture. Individual waveguides are shown, including the placement of delays.

3.10. PR-MESH (1998). The Pipelined Reconfigurable Mesh (PR-Mesh) [7] uses the LARPBS as a building block to make up a k -dimensional mesh. The one dimensional PR-MESH is identical to LARPBS. For the k dimension, each processor has $2k$ ports connected to buses. It uses the CP addressing technique. The bus cycle is described as the end-to-end propagation delay as presented in APPB and LARPBS. In the two dimensional mesh, each processor controls four sets of switches, one set for each intersection of the buses. These switches can be configured in one of ten different ways. This allows traffic to flow differently between a total of four different transmitting segments and four different receiving segments. Figure 3.12 illustrates this architecture. Individual waveguides are shown, including the placement of delays. Papers that report on PR-MESH are [7, 106, 28, 29].

4. Historical Analysis. Some analysis was conducted on the models found in the literature. It includes observations about comparisons between the models, the types of algorithms proposed, the popularity of the models, trends in architecture complexity of the models and some miscellaneous observations of interest.

Theoretical comparisons between several of the optical bus models as well as with respect to PRAM have been published. These comparisons seek to establish both the functional equivalence and the relative strengths of models. Several comparisons are reported in [6]: AROB is compared with reconfigurable networks; and, APPB is compared with PRAM. LARPBS is compared with PRAM in [83]. The authors in [7] compare the PR-MESH model with other reconfigurable models on the basis of complexity classes. One interesting result is "... the contribution of pipelining to the [PR-MESH] model is limited to no more than duplicating buses in the [Linear Reconfigurable Network]. ..." The equivalence of LPB, POB, and LARPBS is reported in [33]. And, the algorithm complexities of the PR-Mesh, APPBS, and AROB are determined to be same as for the LR-Mesh and CF-LR-Mesh [29]. Additional comparison of the PR-MESH with the linear reconfigurable mesh appears in [107]. Some limited architectural comparisons are also made in [32].

Many of the papers surveyed describe algorithms for the respective models. In several cases, see for example [6, 63, 32], communication and computation algorithms are developed as primitives to be used in more sophisticated algorithms. These include binary prefix sums and compaction. In [71], some of these primitives for the LARPBS model are formalized in a lemma. In general, algorithms that have been developed include sorting and selection, matrix calculations (including the Four Russians' algorithm for boolean matrix multiplication), neural networks, and image processing (including vector median filter, Hough transform and the Euclidean Dis-

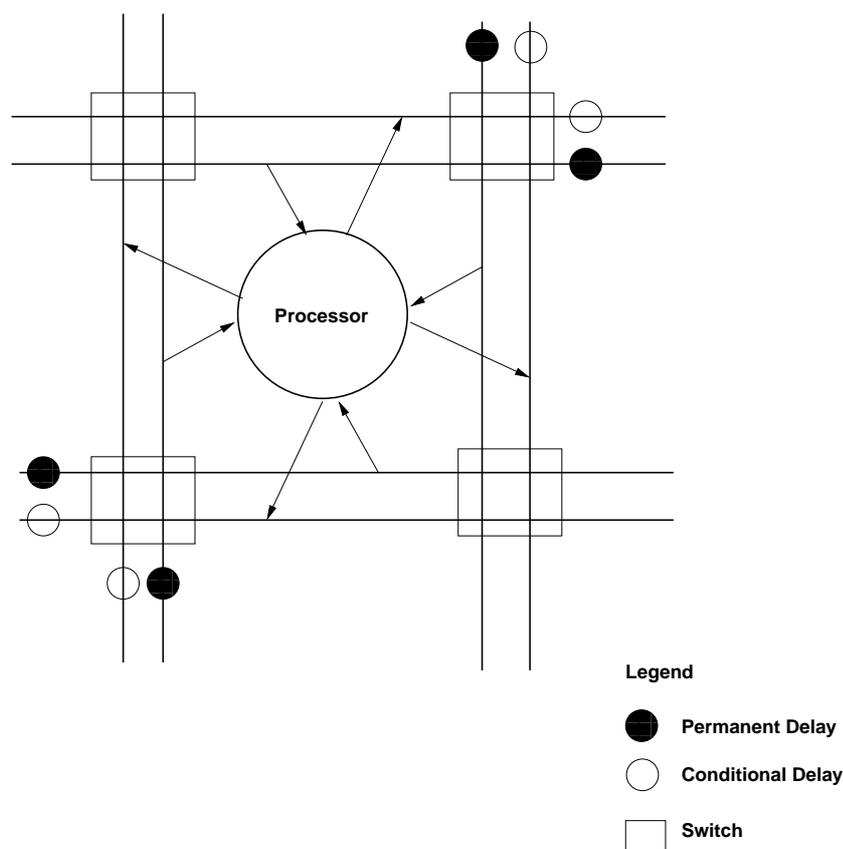


FIG. 3.12. PR-MESH Architecture (1 Node)

tance Transform). Many algorithms exhibit static communication decomposition, that is, the communication pattern is statically determined during algorithm development. This is consistent with both the allocation of communication in terms of bus cycles as well as algorithm development based on primitive operations.

Trends were observed in the popularity of models according to their level of complexity. The analysis included categorizing the number of publications reported per model and per year. Refer to Table 4.1 for the complete list of models and number of publications. In judging the complexity, or sophistication, of a model, the following features are considered: multiple dimensionality, the use of a folded bus, the use of switches, the use of coincident pulse addressing, and bus partitioning. The greater number of these features that a model contains, the more complex and sophisticated it is considered. This informal criterion is used to guide the trend analysis.

From 1990 to 1993, an increase in the sophistication and complexity of the early models is observed. This was followed by a period of simplification (1993-1995). A jump in the sophistication is noted in 1995 with the AROB model. Again, a period of simplification follows (1996-1998) with another jump noted for the PR-MESH model. It is noted that this analysis is consistent with the intention of RASOB as stated in Section 3.5, that is, RASOB was designed to have fewer complexities than ASOS.

The popularity of these models is observable from the number of publications listed in Table 4.1 (some publications are common to two or more models). The three most popular are: RASOB, AROB and LARPBS.

Combining these results, it is suggested that researchers are more strongly attracted to something between the simple and the complicated. It is also suggested that the capabilities incorporated into the models during the middle period, 1995-1996, are sufficient for supporting current research interests. It is worthy to point out that the recent PR-MESH model may indeed signify a future research movement to consider models of higher degrees of sophistication and complexity. If so, then this may also indicate that current research has explored many of the issues of the optical bus parallel model and is ready to consider additional challenges. However, these latter comments must be interpreted as highly speculative given the lack of data to support such a trend.

TABLE 4.1
Model Publications

Model	Number of Publications	Year of First Publication
APPB	10	1990
APPBS	6	1990
ASOS	1	1993
LPB	4	1994
RASOB	10	1995
AROB	23	1995
LARPBS	46	1996
POB	5	1997
LAPOB	1	1998
PR-MESH	4	1998

Perhaps in several years, additional publication history could support or refute such speculation.

During the course of this analysis, several other interesting observations were noted. One publication reporting work on ASOS was located, yet, it is cited in many publications. Some papers claim that to provide for MIMD algorithms, additional complexities would need to be incorporated. Other optical buses can be found in the literature, for example, free space optical buses as well as NASA's ROBUS as part of the SPIDER architecture. These models do not appear to follow the architectural approach of the models surveyed in this paper and therefore were not included into this paper.

Some recent developments are: a) the restricted LARPBS (RLARPBS) model [99] proposed to more accurately model time analysis of algorithms, b) the parameterized LARPBS (LARPBS(p)) model [103] proposed as a bridging model and c) a generic optical bus model [108] proposed to capture some of the common features of the models surveyed in this paper for MIMD communication analysis.

5. Bus Cycle Issues. In the course of the analysis, bus cycles have been noted to play a crucial role in the algorithmic evaluations on these models. In many cases, algorithm complexity is described as order Omega of bus cycle, for example, constant time bus cycle complexity for the binary prefix sums algorithm on the LARPBS. Closer examination of bus cycle definitions on many of the models reveal inconsistencies between the architecture and the definition, that is, the definition appears to represent a simplified architecture. Investigating this further, it is noted that nearly all of the algorithmic work referencing bus cycle is given in the context of asymptotic analysis expressions, wherein only the dominate term needs to be expressed. Although not in all cases, it is noted that the definitions as given in the literature are consistent with such a use.

A refinement of the bus cycle definitions for all the models is presented in this section. A general expression template is formulated which is then applied to each architecture. In general, the folded bus cycle equation is composed of four parts. Part 1 of the equation corresponds to the length of the transmitting and receiving portions of the folded bus. Part 2 corresponds to the curved portion of the bus, while Part 3 corresponds to the delays on the bus. Part 4 corresponds to the portion of the bus that remains past the detection point of the last processor on the receiving side of the bus. Recall from Section 2 that $b\omega < \tau$. To efficiently use the bus bandwidth, $b\omega$ should be maximized. To model this requirement, the factor $\tau - \epsilon$ is introduced, and may be approximated as simply τ . Table 5.1 presents the refined bus cycle definitions as compared with those given in the literature for each of the models. In the Refined Bus Cycle column, 's', 'r' and 'm' refer to the select, reference and message waveguides, respectively.

Note that, in cases where the model is only 2-D, one of the 1-D 'pieces' is used to compute the bus cycle; in cases where the model is 1-D or multidimensional, the 1-D variety is used. On the PR-MESH, this is for $k = 1$ (the 1-D case). S_i denotes each of the conditional delays, where $S_i = 0$ means the delay controlled by P_i is turned off and $S_i = 1$ means the delay is turned on. The processor time component is denoted by ϕ . For ASOS, we interpret the D parameter in terms of the corresponding time parameter τ .

TABLE 5.1
Bus Cycle Equations

Model	Literature Bus Cycle	Refined Bus Cycle
APPB	$N\tau$	$(N+1)\tau$
APPBS	$N\tau$	$(N+1)\tau$
ASOS	$2(N-1)\tau$	$2(N-1)\tau + \gamma + \tau + \phi$
RASOB	$2N\tau$	$2(N-1)\tau + \gamma + \tau$
LPB	$2N\tau + (N-1)\omega$	s: $2(N-1)\tau + \gamma + \omega \sum S_i + \tau$ r,m: $2(N-1)\tau + \gamma + (N-1)\omega + \tau$
AROB	$2N\tau + \phi$	s: $2(N-1)\tau + \gamma + \tau$ r,m: $2(N-1)\tau + \gamma + (N-1)\omega + \tau + \phi$
LARPBS	$2N\tau + (N-1)\omega$	s: $2(N-1)\tau + \gamma + \omega \sum S_i + \tau$ r,m: $2(N-1)\tau + \gamma + (N-1)\omega + \tau$
POB	N/A	s,m: $2(N-1)\tau + \gamma + \tau$ r: $2(N-1)\tau + \gamma + \omega \sum S_i + \tau$
LAPOB	N/A	s: $2(N-1)\tau + \gamma + \tau$ r,m: $2(N-1)\tau + \gamma + (N-1)\omega + \tau$
PR-MESH	see APPB & LARPBS	s: $2(N-1)\tau + \gamma + \omega \sum S_i + \tau$ r,m: $2(N-1)\tau + \gamma + (N-1)\omega + \tau$

6. Conclusions. This paper provides a comprehensive overview and survey of the developments in optical bus parallel computing models. The first model proposed was in 1990 and since then, ten distinct parallel computing models have been proposed.

Specifically, the research trends we have observed indicate periods of model development leading to more and more sophistication and complexity in the model, followed by periods of model simplifications. These periods occur in cycles. With the many publications surveyed, we note the widespread and global research interest in these models. The three most popular models appears to be RASOB, AROB and LARPBS. We also have analyzed a crucial aspect of these models, the bus cycle time definitions. We have determined inaccuracies in most of the definitions appearing in the literature, although, for most of the applications such definitions have been used for, these inaccuracies appear not to be significant. In the interests of clarifying the correct definitions as well as to support our current research work, we have also provided refinements to the bus cycle definitions.

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REFERENCES

- [1] S. Sahni, "Models and algorithms for optical and optoelectronic parallel computers," *International Journal of Foundations in Computer Science*, vol. 12, pp. 249–264, June 2001.
- [2] S. Sahni, "Models and algorithms for optical and optoelectronic parallel computer," in *proc. of 1999 International Symposium on Parallel Architecture, Algorithms and Networks (I-SPAN'99)*, pp. 2–7, June 1999.
- [3] Z. Guo, R. G. Melhem, R. W. Hall, D. M. Chiarulli, and S. P. Levitan, "Array processors with pipelined optical busses," in *Proc. 3rd Symposium on Frontiers of Massively Parallel Computation (Cat. No.90CH2908-2)* (J. Jaja, ed.), (College Park, MD, USA), pp. 333–342, October 1990.
- [4] C. Qiao and R. G. Melhem, "Time-division optical communications in multiprocessor arrays," *IEEE Transactions on Computers*, vol. 42, pp. 577–590, May 1993.
- [5] C. Qiao, "Efficient matrix operations in a reconfigurable array with spanning optical busses," in *Proceedings. Frontiers '95. The Fifth Symposium on the Frontiers of Massively Parallel Computation (Cat. No.95TH8024)*. IEEE Comput. Soc. Press, 1994, (McLean, VA, USA), pp. 273–280, Feb 1995.
- [6] S. Pavel and S. G. Akl, "On the power of arrays with reconfigurable optical busses," *Technical Report No. 95-374*, Queens University, Kingston, Ontario, CANADA, February 1995.
- [7] J. L. Trahan, A. G. Bourgeois, and R. Vaidyanathan, "Tighter and broader complexity results for reconfigurable models," *Parallel Processing Letters*, vol. 8, no. 3, pp. 271–282, 1998.

- [8] Y. Pan, "Order statistics on optically interconnected multiprocessor systems," *Optics and Laser Technology*, vol. 26, pp. 281–287, August 1994.
- [9] Y. Pan and M. Hamdi, "Quicksort on a linear array with a reconfigurable pipelined bus system," in *Proc. of the IEEE International Symposium on Parallel Architectures, Algorithms, and Networks*, pp. 313–319, June 1996.
- [10] Y. Li, Y. Pan, and S. Zheng, "A pipelined TDM optical bus with conditional delays," in *Proceedings of the Fourth International Conference on Massively Parallel Processing Using Optical Interconnections* (J. Goodman, S. Hinton, T. Pinkston, and E. Schenfeld, eds.), (Montreal, Canada), pp. 196–201, June 1997.
- [11] H. ElGindy, "An improved sorting algorithm for linear arrays with optical buses (extended abstract)," (*Manuscript*), April 1998.
- [12] D. M. Chiarulli, R. G. Melhem, and S. P. Levitan, "Using coincident optical pulses for parallel memory addressing," *IEEE Computer*, vol. 20, pp. 48–58, Dec. 1987.
- [13] S. Zheng, K. Li, Y. Pan, and M. C. Pinotti, "Generalized coincident pulse technique and new addressing schemes for time-division multiplexing optical buses," *Journal of Parallel and Distributed Computing*, vol. 61, pp. 1033–1051, August 2001.
- [14] C. Qiao, R. G. Melhem, D. M. Chiarulli, and S. F. Levitan, "Optical multicasting in linear arrays," *International Journal of Optical Computing*, vol. 2, pp. 31–48, April 1991.
- [15] S. Zheng and Y. Li, "Pipelined asynchronous time-division multiplexing optical bus," *Optical Engineering*, vol. 36, pp. 3392–3400, December 1997.
- [16] S. Zheng, , and Y. Li, "A pipelined TDM optical bus with improved performance," in *Proceedings. Third International Symposium on Parallel Architectures, Algorithms, and Networks (I-SPAN '97)* (F. Lai, B. Maggs, and D. Hsu, eds.), (Taipei, Taiwan), pp. 49–55, December 1997.
- [17] S. Q. Zheng, K. Li, Y. Pan, and M. C. Pinotti, "New addressing schemes for pipelined optical buses," in *6th International Conference on Parallel Interconnects (PI'9)* (M. Haney, R. Kostuk, C. Lund, and E. Schenfield, eds.), (Anchorage, AK, USA), pp. 230–237, October 1999.
- [18] Z. Guo, "Sorting on array processors with pipelined buses," in *Proceedings of the 1992 International Conference on Parallel Processing*, pp. 280–292, 1992. Vol. 3.
- [19] Z. Guo, R. Melhem, R. Hall, D. Chiarulli, and S. Levitan, "Pipelined communications on optical busses," in *Proceedings of Spie—the International Society for Optical Engineering*, (Boston, MA, USA), pp. 415–426, Nov 1990.
- [20] Z. Guo and R. G. Melhem, "Embedding pyramids in array processors with pipelined busses," in *Proceedings of the International Conference on Application Specific Array Processors (Cat. No.90CH2920-7)* (S.-Y. Kung, E. Swartzlander, J. Fortes, and K. Przytula, eds.), (Princeton, NJ, USA), pp. 665–676, September 1990.
- [21] G. Zicheng, R. Melhem, R. Hall, D. Chiarulli, and S. Levitan, "Pipelined communications on optical busses," in *Proc. of Spie*, pp. 415–26, 1991.
- [22] Z. Guo, R. G. Melhem, R. W. hall, D. M. Chiarulli, and S. P. Levitan, "Pipelined communications in optically interconnected arrays," *Journal of Parallel and Distributed Computing*, vol. 12, pp. 269–282, 1991.
- [23] Z. Guo, "Optically interconnected processor arrays with switching capability," *Journal of Parallel and Distributed Computing*, vol. 23, pp. 314–329, December 1994.
- [24] G. Zicheng, "Optically interconnected processor arrays with switching capability," *Journal of Parallel & Distributed Computing*, vol. 23, pp. 314–29, Dec. 1994.
- [25] S. Pavel and S. G. Akl, "On the power of arrays with optical pipelined buses," in *Proc. of the International Conference on Parallel and Distributed Processing Techniques and Applications (PDPTA'96)*, Vol. III (H. Arabnia, ed.), (Sunnyvale, California, USA), pp. 1443–1453, August 1996.
- [26] M. Hamdi, C. Qiao, and Y. Pan, "On the computing power of arrays of processors with optical pipelined buses," *Parallel Processing Letters*, vol. 8, pp. 503–513, Dec. 1998.
- [27] M. Middendorf and H. ElGindy, "Matrix multiplication on processor arrays with optical buses," *Informatica*, vol. 22, pp. 255–62, Oct. 1998.
- [28] A. Bourgeois and J. Trahan, "Relating two-dimensional reconfigurable meshes with optically pipelined buses," in *Proceedings 14th International Parallel and Distributed Processing Symposium (IPDPS 2000)*, (Los Alamitos, CA, USA), pp. 747–52, May 2000.
- [29] A. Bourgeois and J. Trahan, "Relating two-dimensional reconfigurable meshes with optically pipelined buses," *International Journal of Foundations of Computer Science*, vol. 11, pp. 553–71, Dec. 2000.
- [30] Y. Li, J. Tao, and S. Zheng, "A symmetric processor array with synchronous optical buses and switches," *Parallel Processing Letters*, vol. 8, no. 3, pp. 283–295, 1998.
- [31] Y. Pan, "Order statistics on a linear array with a reconfigurable bus," *Future Generation Computer Systems*, vol. 11, pp. 321–328, June 1995.
- [32] Y. Pan, "Basic data movement operations on the LARPBS model," in *Parallel Computing Using Optical Interconnections* (K. Li, Y. Pan, and S.-Q. Zheng, eds.), pp. 227–247, Kluwer Academic Publishers, 1998.
- [33] J. L. Trahan, A. G. Bourgeois, Y. Pan, and R. Vaidyanathan, "Optimally scaling permutation routing on reconfigurable linear arrays with optical buses," *Journal of Parallel and Distributed Computing*, vol. 60, pp. 1125–1136, September 2000.
- [34] J. L. Trahan, A. G. Bourgeois, Y. Pan, and R. Vaidyanathan, "Optimally scaling permutation routing on reconfigurable linear arrays with optical buses," in *Second Merged Symposium IPPS/SPDP, 13th International Parallel Processing Symposium & 10th Symposium on Parallel and Distributed Processing*, (San Juan, Puerto Roco), April 1999.
- [35] M. Hamdi, "Enhanced mesh-connected computers for image processing applications," in *Proceedings. CAMP '95 Computer Architectures for Machine Perception (Cat. No.95TB8093)*. *IEEE Comput. Soc. Press. 1995* (V. Cantoni, L. Lombardi, M. Mosconi, M. Savini, and A. Setti, eds.), (Como, Italy), pp. 375–383, Sept 1995.
- [36] C. Qiao, "On designing communication-intensive algorithms for a spanning optical bus based array," *Parallel Processing Letters*, vol. 5, no. 3, pp. 499–511, 1995.

- [37] M. Hamdi, J. Tong, and C. Kin, "Fast sorting algorithms on reconfigurable array of processors with optical buses," in *Proceedings. 1996 International Conference on Parallel and Distributed Systems (Cat. No.96TB100045)*. IEEE Comput. Soc. Press, 1996, (Tokyo, Japan), pp. 183–188, June 1996.
- [38] M. Hamdi and Y. Pan, "Communication-efficient algorithms on reconfigurable array of processors with spanning optical buses," in *Proceedings. Second International Symposium on Parallel Architectures, Algorithms, and Networks (I-SPAN '96) (Cat. No.96TB100044)*. IEEE Comput. Soc. Press, 1996 (G.-J. Li, D. Hsu, S. Horiguchi, and B. Maggs, eds.), (Beijing, China), pp. 440–446, June 1996.
- [39] Y. Mei and Chunming-Qiao, "Embedding binary trees in arrays with optical busses," in *Proceedings of the Fourth International Conference on Massively Parallel Processing Using Optical Interconnections* (J. Goodman, S. Hinton, T. Pinkston, and E. Schenfeld, eds.), (Montreal, Canada), June 1997.
- [40] C. Qiao, "A unique design of fiber-optic interconnection networks and algorithms," in *Parallel Computing Using Optical Interconnections* (K. Li, Y. Pan, and S.-Q. Zheng, eds.), pp. 163–184, Kluwer Academic Publishers, 1998.
- [41] C. Qiao and Y. Mei, "An improved embedding of binary trees in a square reconfigurable array with spanning optical buses," *Parallel Processing Letters*, vol. 8, no. 3, pp. 321–336, 1998.
- [42] M. Hamdi, C. Qiao, Y. Pan, and J. Tong, "Communication-efficient sorting algorithms on reconfigurable array of processors with slotted optical buses," *Journal of Parallel and Distributed Computing*, vol. 57, pp. 166–187, May 1999.
- [43] Y. Mei and C. Qiao, "An efficient embedding of binary trees in reconfigurable arrays with spanning optical buses," *International Journal of Distributed Systems & Networks*, vol. 2, no. 1, pp. 40–48, 1999.
- [44] S. Pavel and S. Akl, "Integer sorting and routing in arrays with reconfigurable optical buses," in *Proceedings of 25th International Conference on Parallel Processing* (A. Bojanczyk, ed.), (Ithaca, NY, USA), pp. 90–94, Aug 1996.
- [45] S. Rajasekaran and S. Sahni, "Sorting and routing on the array with reconfigurable optical buses," in *Proc. 1996 IEEE 2ed International Conference on Algorithms and Architectures for Parallel Processing (ICA3PP'96)*, (Singapore), June 1996.
- [46] S. Pavel and S. Akl, "Integer sorting and routing in arrays with reconfigurable optical buses," in *Proceedings of the International Conference on Parallel Processing*, (Bloomington, Illinois), pp. 90–94, August 1996. volume 2.
- [47] S. Pavel and S. Akl, "Efficient algorithms for the hough transform on arrays with reconfigurable optical buses," in *Proceedings of the International Parallel Processing Symposium*, (Maui, Hawaii), pp. 697–701, April 1996.
- [48] S. Pavel and S. Akl, "Matrix operations using arrays with reconfigurable optical buses," *Journal of Parallel Algorithms and Applications*, vol. 8, pp. 223–242, 1996.
- [49] S. Rajasekaran and S. Sahni, "Deterministic routing on the array with reconfigurable optical buses," *Parallel Processing Letters*, vol. 7, pp. 219–224, Sept 1997.
- [50] S. Rajasekaran and S. Sahni, "Computing on the array with reconfigurable optical buses," in *World Multiconference on Systemics, Cybernetics, and Informatics*, (Caracas, Venezuela), pp. 459–466, 1997.
- [51] S. Rajasekaran and S. Sahni, "Sorting, selection, and routing on the array with reconfigurable optical buses," *IEEE Transactions on Parallel & Distributed Systems*, vol. 8, pp. 1123–32, Nov. 1997.
- [52] S. Pavel and S. Akl, "Integer sorting and routing in arrays with reconfigurable optical buses," *International Journal of Foundations of Computer Science, Special Issue on Interconnection Networks*, vol. 9, pp. 99–120, March 1998.
- [53] S. D. Pavel and S. G. Akl, "Computing the hough transform on arrays with reconfigurable optical buses," in *Parallel Computing Using Optical Interconnections* (K. Li, Y. Pan, and S.-Q. Zheng, eds.), pp. 205–226, Kluwer Academic Publishers, 1998.
- [54] S. Rajasekaran and S. Sahni, "Fundamental algorithms for the array with reconfigurable optical busses," in *Parallel Computing Using Optical Interconnections* (K. Li, Y. Pan, and S.-Q. Zheng, eds.), pp. 185–204, Kluwer Academic Publishers, 1998.
- [55] C.-H. Wu, S.-J. Horng, and H.-R. Tsai, "Template matching on arrays with reconfigurable optical buses," in *Operations Research and its Applications. Third International Symposium (ISORA'98)* (D.-Z. Du, X.-S. Zhang, and K. Cheng, eds.), (Kunming, China), Aug. 1998.
- [56] H. Elgindy and S. Rajesekaran, "Sorting and selection on a linear array with optical bus system," *Parallel Processing Letters*, vol. 9, pp. 373–383, Sept 1999.
- [57] C.-H. Wu, S.-J. Horng, and H.-R. Tsai, "Efficient parallel algorithms for hierarchical clustering on arrays with reconfigurable optical buses," *Journal of Parallel & Distributed Computing*, vol. 60, pp. 1137–53, Sept 2000.
- [58] C.-H. Wu, S.-J. Horng, H.-R. Tsai, J.-F. Lin, and T.-L. Lin, "An optimal parallel algorithm for computing moments on arrays with reconfigurable optical buses," in *Proc. 14th International Parallel and Distributed Processing Symposium (IPDPS 2000)*, (Los Alamitos, CA, USA), pp. 741–6, May 2000.
- [59] C.-H. Wu, S.-J. Horng, Y.-R. Wang, and L.-G. Jeng, "Parallel algorithms for vector median filtering," in *Proceedings of the 4th International Conference on Algorithms and Architectures for Parallel Processing*, pp. 240–51, 2000.
- [60] C.-H. Wu and S.-J. Horng, "L/sub 2/ vector median filters on arrays with reconfigurable optical buses," *IEEE Transactions on Parallel and Distributed Systems*, vol. 12, no. 12, pp. 1281–92, Dec. 2001.
- [61] C.-H. Wu and S.-J. Horng, "Scalable and optimal speed-up parallel algorithms for template matching on arrays with reconfigurable optical buses," *International Journal of Foundations of Computer Science*, vol. 14, no. 1, pp. 79–98, Feb. 2003.
- [62] C.-H. Wu and S.-J. Horng, "Fast and scalable selection algorithms with applications to median filtering," *IEEE Transactions on Parallel and Distributed Systems*, vol. 14, pp. 983–92, Oct. 2003.
- [63] Y. Pan and K. Li, "Linear array with a reconfigurable pipelined bus system — concepts and applications," in *Proc. of the International Conference on Parallel and Distributed Processing Techniques and Applications (PDPTA'96)*, Vol. III (H. Arabnia, ed.), (Sunnyvale, California, USA), pp. 1431–1441, August 1996.
- [64] R. Roldan and B. J. d'Auriol, "A preliminary feasibility study of the LARPBS optical bus parallel model," in *Proceedings of the 17th International Symposium on High Performance Computing Systems and Applications (HPCS 2003) and OSCAR Symposium* (D. Senechal, ed.), (Sherbrooke, Quebec, Canada), pp. 181–188, May 2003.

- [65] H. Kimm, "Inversion number algorithm on a linear array with a reconfigurable pipelined bus system," in *Proc. of the International Conference on Parallel and Distributed Processing Techniques and Applications (PDPTA'96)*, Vol. III (H. Arabnia, ed.), (Sunnyvale, California, USA), pp. 1398–1407, August 1996.
- [66] Y. Pan, K. Li, and S.-Q. Zheng, "Fast nearest neighbor algorithms on a linear array with a reconfigurable pipelined bus system," in *Proceedings. Third International Symposium on Parallel Architectures, Algorithms, and Networks (I-SPAN '97) (Cat. No.97TB100209)*. *IEEE Comput. Soc. 1997* (F. Lai, B. Maggs, and D. Hsu, eds.), (Taipei, Taiwan), pp. 444–450, Dec 1997.
- [67] B. Cong, "On embeddings of neural networks into massively parallel computer systems," in *Proceedings of the IEEE 1997 National Aerospace and Electronics Conference. NAICON 1997.*, (Dayton, OH), pp. 231–238, July 1997.
- [68] J. L. Trahan, Y. Pan, R. Vaidyanathan, and A. G. Bourgeois, "Scalable basic algorithms on a linear array with a reconfigurable pipelined bus system," in *10th International Conference on Parallel and Distributed Computing Systems*, (New Orleans, LA, USA), pp. 564–569, 1997.
- [69] H. Kimm, "Parallel total weight crossing number algorithm for channel routing on a linear array with a reconfigurable pipelined bus system," in *Proceedings of the Twenty-Ninth Southeastern Symposium on System Theory (Cat. No.97TB100097)*. *IEEE Comput. Soc. Press. 1997*, (Cookeville, TN, USA), pp. 183–187, March 1997.
- [70] K. Li, "Boolean matrix multiplication on a linear array with a reconfigurable pipelined bus system," in *Proc. of the 11th Annual International Symposium on High Performance Computing Systems (HPCS'97)*, (Winnipeg, Manitoba, Canada), pp. 179–190, July 1997.
- [71] K. Li, "Constant time boolean matrix multiplication on a linear array with a reconfigurable pipelined bus system," *Journal of Supercomputing*, vol. 11, no. 4, pp. 391–403, 1997.
- [72] K. Li, Y. Pan, and S.-Q. Zheng, "Scalable parallel matrix multiplication using reconfigurable pipelined optical bus systems," in *Proceedings of the 10th IASTED International Conference on Parallel and Distributed Computing and Systems* (Y. Pan, S. G. Akl, and K. Li, eds.), (Las Vegas, Nevada, USA), pp. 238–243, Oct. 1998.
- [73] K. Li, Y. Pan, and S.-Q. Zheng, "Fast and efficient parallel matrix computations on a linear array with a reconfigurable pipelined optical bus system," in *Proceedings of HPCS '98: 12th Annual International Symposium on High Performance Computing Systems* (J. Schaeffer, ed.), (Calgary, Alta., Canada), pp. 363–380, May 1998.
- [74] Y. Pan, M. Hamdi, and K. Li, "Efficient and scalable quicksort on a linear array with a reconfigurable pipelined bus system," *Future Generations Computer Systems*, vol. 13, pp. 501–513, May 1998.
- [75] Y. Pan and K. Li, "Linear array with a reconfigurable pipelined bus system. concepts and applications," *Information Sciences*, vol. 106, pp. 237–258, May 1998.
- [76] K. Li, "Fast matrix multiplication and related operations using reconfigurable optical busses," in *Parallel Computing Using Optical Interconnections* (K. Li, Y. Pan, and S.-Q. Zheng, eds.), pp. 248–273, Kluwer Academic Publishers, 1998.
- [77] K. Li, Y. Pan, and S. Q. Zheng, "Fast and processor efficient parallel matrix multiplication algorithms on a linear array with a reconfigurable pipelined bus system," *IEEE Transactions on Parallel and Distributed Systems*, vol. 9, pp. 705–720, August 1998.
- [78] Y. Pan, K. Li, and S.-Q. Zheng, "Fast nearest neighbor algorithms on a linear array with a reconfigurable pipelined bus system," *Parallel Algorithms and Applications*, vol. 13, pp. 1–25, 1998.
- [79] K. Li, Y. Pan, and S. Zheng, "Parallel matrix computations using a reconfigurable pipelined optical bus," *Journal of Parallel & Distributed Computing*, vol. 59, pp. 13–30, Oct 1999.
- [80] Y. Han, Y. Pan, and H. Shen, "Fast parallel selection on the linear array with reconfigurable pipelined bus system," in *Proceedings. Frontiers '99. Seventh Symposium on the Frontiers of Massively Parallel Computation. IEEE Comput. Soc. 1999*, (Annapolis, MD, USA), pp. 286–293, Feb 1999.
- [81] K. Li and V. Pan, "Parallel matrix multiplication on a linear array with a reconfigurable pipelined bus system," in *Proceedings 13th International Parallel Processing Symposium and 10th Symposium on Parallel and Distributed Processing. IPPS/SPDP 1999*, (San Juan, Puerto Rico), pp. 31–35, April 1999.
- [82] K. Li, Y. Pan, and M. Hamdi, "Solving graph theory problems using reconfigurable pipelined optical buses," in *Parallel and Distributed Processing. 11th IPPS/SPDP'99 Workshops held in conjunction with the 13th International Parallel Processing Symposium and the 10th Symposium on Parallel and Distributed Processing*, (San Juan, Puerto Rico), pp. 911–923, April 1999.
- [83] K. Li, Y. Pan, and S. Zheng, "Efficient deterministic and probabilistic simulations of PRAMs on linear arrays with reconfigurable pipelined bus systems," *Journal of Supercomputing*, vol. 15, pp. 163–181, Feb 2000.
- [84] B. J. d'Auriol, "Communication in the LARPBS (optical bus) model: A case study," in *Proc. of The Fourth International Conference on Algorithms And Architecture for Parallel Processing (ICA3PP2000)* (A. G. et al., ed.), (Hong Kong), pp. 581–590, December 2000.
- [85] A. Datta and S. Soundaralakshmi, "Computing connected components on a linear array with a reconfigurable pipelined bus system," in *Proceedings of PART2000. Seventh Australasian Conference on Parallel and Real-Time Systems* (H. ElGindy and C. Fidge, eds.), (Sydney, NSW, Australia), pp. 181–191, Nov 2000.
- [86] K. Li, Y. Pan, and M. Hamdi, "Solving graph theory problems using reconfigurable pipelined optical buses," *Parallel Computing*, vol. 26, pp. 723–735, May 2000.
- [87] M. He and S. Q. Zheng, "An optimal sorting algorithm on a linear array with reconfigurable pipelined bus system," in *PDCS 2002: 15th International Conference on Parallel and Distributed Computing Systems*, pp. 386–91, 2002.
- [88] A. Datta and Soundaralakshmi, "Fast and scalable algorithms for the euclidean distance transform on the larpbs," in *Proceedings of IPDPS Workshop on Advances in Parallel and Distributed Computational Models*, (San Francisco), April 2001.
- [89] K. Li and V. Y. Pan, "Parallel matrix multiplication on a linear array with a reconfigurable pipelined bus system," *IEEE Transactions on Computers*, vol. 50, pp. 519–525, May 2001.
- [90] A. Datta, "Efficient graph algorithms on a linear array with a reconfigurable pipelined bus system," in *Proceedings of IEEE International Symposium on Parallel and Distributed Processing*, (San Francisco, CA, USA), April 2001.

- [91] K. Li, "Fast and scalable parallel algorithms for matrix chain product and matrix powers on reconfigurable pipelined optical buses," *Journal of Information Science and Engineering*, vol. 18, pp. 713–727, Sept 2002.
- [92] Y. Pan, Y. Li, J. Li, K. Li, and S. Zheng, "Efficient parallel algorithms for distance maps of 2d binary images using an optical bus," *IEEE Transactions on Systems, Man, and Cybernetics - Part A: Systems and Humans*, vol. 32, pp. 228–236, March 2002.
- [93] Y. Pan, Y. Li, J. Li, K. Li, and S. Zheng, "Efficient parallel algorithms for distance maps of 2d binary images using an optical bus," *IEEE Transactions on Systems, Man, and Cybernetics - Part A: Systems and Humans*, vol. 32, pp. 228–236, March 2002.
- [94] A. Datta, "Efficient graph-theoretic algorithms on a linear array with a reconfigurable pipelined bus system," *Journal of Supercomputing*, vol. 23, pp. 193–211, Sept 2002.
- [95] A. Datta, S. Soundaralakshmi, and R. Owens, "Fast sorting algorithms on a linear array with a reconfigurable pipelined bus system," *IEEE Transactions on Parallel and Distributed Systems*, vol. 13, pp. 212–222, March 2002.
- [96] Y. Han, Y. Pan, and H. Shen, "Sublogarithmic deterministic selection on arrays with a reconfigurable optical bus," *IEEE Transactions on Computing*, vol. 51, pp. 702–707, June 2002.
- [97] J. Li, Y. Pan, and H. Shen, "More efficient topological sort using reconfigurable optical buses," *The Journal of Supercomputing*, vol. 24, pp. 251–258, March 2003.
- [98] H. Kimm and D. Semé, "Longest repeated suffix problem on the arrays with pipelined optical bus systems," in *Proceedings of the 35th Southeastern Symposium on System Theory*, (Morgantown, WV, USA), pp. 69–73, March 2003.
- [99] Y. Pan, "Computing on the restricted LARPBS model," in *Proc. of The 2003 International Symposium on Parallel and Distributed Processing and Applications*, (Aizu-Wakamatsu City, Japan), pp. 9–13, July 2003. Lecture Notes in Computer Science, vol. 2745.
- [100] A. G. Bourgeois and J. L. Trahan, "Fault tolerant algorithms for a linear array with a reconfigurable pipelined bus system," *Parallel Algorithms and Applications*, vol. 18, pp. 139–153, September 2003.
- [101] L. Chen, Y. Pan, and X. Xu, "Scalable and efficient parallel algorithms for euclidean distance transform on the LARPBS model," *IEEE Transactions on Parallel and Distributed Systems*, to appear, 2004.
- [102] L. Chen, H. Chen, Y. Pan, and Y. Chen, "A fast efficient parallel hough transform algorithm on LARPBS," *The Journal of Supercomputing*, vol. 29, pp. 185–195, 2004.
- [103] B. J. d'Auriol and R. Molakaseema, "A parameterized linear array with a reconfigurable pipelined bus system: LARPBS(p)," *The Computer Journal*, vol. 48, no. 1, pp. 115–125, 2005.
- [104] A. Datta and S. Soundaralakshmi, "Fast and scalable algorithms for the euclidean distance transform on a linear array with a reconfigurable pipelined bus system," *Journal of Parallel and Distributed Computing*, vol. 64, no. 3, pp. 360–369, 2004.
- [105] Y. Li, Y. Pan, and S. Zheng, "Pipelined time-division multiplexing optical bus with conditional delays," *Optical Engineering*, vol. 36, pp. 2417–2424, September 1997.
- [106] J. Fernandez-Zepeda, R. Vaidyanathan, and J. Trahan, "Improved scaling simulation of the general reconfigurable mesh," in *Proceedings. Parallel and Distributed Processing, 11 IPPS/SPDP'99 Workshops*, (San Juan, Puerto Rico), pp. 615–624, April 1999.
- [107] J. Fernandez-Zepeda, R. Vaidyanathan, and J. Trahan, "Using bus linearization to scale the reconfigurable mesh," *Journal of Parallel and Distributed Computing*, vol. 62, pp. 495–516, April 2002.
- [108] B. J. d'Auriol and M. Beltran, "Optical bus communication modeling and simulation," in *Proc. of the International Symposium on High Performance Computing Systems and Applications (HPCS 2004)* (M. R. Eskicioglu, ed.), (Winnipeg, Manitoba, Canada), pp. 135–142, May 2004.

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