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HIGH SPEED LOW POWER ANALYSIS OF 12 TRANSISTORS 2×4 LINE DECODER USING 45GPDK TECHNOLOGY

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Abstract. This paper proposes the high speed low power analysis of 12 transistors 2×4 Low Power (LP) and Low Power Inverting (LPI) Decoders by using Dual Value Logic (DVL) and Complementary Metal Oxide Semiconductor (CMOS) Logic. A huge challenge faced by this era of developing is power reduction. The LP circuit design is a requesting issue in high performance digital frameworks, for example, microchips, DSPs and other different applications. Power and speed are the main highlights considered while comparing any design. Diminishing chip area is additionally truly impressive factor, designers need to recall when suggesting any novel design. 2×4 LP and LPI Decoders using 12T (Transistor) is used for conversion of binary inputs to associated output bits in a pattern. A novel design (CMOS logic and DVL logic) of 2×4 LP and LPI Decoders using 12T is proposed with area optimization, LP and high speed in this paper. Delay and power is evaluated between the novel design and CMOS logic. The novel design of 12T LP and LPI 2×4 Decoders is 60.72% optimized for power in contrast to CMOS logic design at a typical value of 1.8V. The proposed method has been validated using Cadence 45 GPDK (Generic Product Design Key) Virtuoso Tool.

Key words: CMOS and DVL, LP Decoder, LPI Decoder and 12T.

1. Introduction. The bulk integrated circuits consist primarily of logic gates created utilizing static CMOS circuits [1].The pullup PMOS and NMOS pulldown network are the two main components of a CMOS circuit. Display resilience in the face of background noise and device fluctuations, consistent performance at low voltages and small transistor sizes are two advantages of CMOS circuitry [2]. Since CMOS circuits can only accept inputs at the transistor's gate terminals, fewer building blocks are available when synthesizing cell-based logic. To compete with CMOS logic, the 1990s saw the development of Pass Transistor Logic (PTL) [3]. When compared to CMOS logic [4], pass transistor logic has advantages in terms of speed, power, and area. No matter which diffusion terminals of the transistors the inputs are tied to the either source/drain or gate, determines The primary design difference between pass transistor circuits. The two most popular techniques for building pass transistor circuits are, at first the PMOS and NMOS transistors are used. while in the second, a transmission gate is used to combine the two types of transistors in parallel [5].

The requirement for miniaturization and voltage scaling are two examples of how advances in VLSI technology have imposed new requirements on the design of swift, space- saving, and low-power logic systems. For high-performance computing devices like microprocessors and digital signal processors, LP design is a significant challenge. In computing, A straightforward combinational circuit called a decoder that transforms series of input signals into another code. Seven-segment displays, address decoding with in arrays of memory, data de-multiplexing and microchip/microcontroller personal based architectures are just a few of the many uses for line Decoders. Address Decoders are critical components because their design heavily influences consumption of power and access time of the SRAM [6] memory cell. For the sake of lowering the electrical bill, delay, and transistor count when constructing Decoders, a novel mixed logic approach is presented in this study [7].

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Table 2.1: Non-Inverting 2×4 Decoder Truth table

A	**B**	D_0	D_1	D_2	D_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Table 2.2: Inverting 2×4 Decoder Truth table

A	**B**	I_0	I_1	I_2	I_3
0	0	0	1	1	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	1	1	1	0

2. Literature. Binary codes in digital systems are used to represent discrete amounts of information. An n-bit binary code can represent up to n distinct pieces of encoded data. Combining many circuits, a decoder converts binary data from n input lines to a maximum of 2×n different output lines or fewer if the n-bit coded data contains any unused combinations [8]. The circuits were looked at. These decoders are n-to-m line and produce the m = 2×n input variable minterms.

A decoder with 2×4 lines produces four outputs from two inputs. Depending on the corresponding input combinations, there will only one active output at any given time. Table 2.1 summarizes the non-inverting 2×4 decoder's truth table [9], inputs A and B produces $D_0, D_1, D_2 \& D_3$ as outputs .The complimentary outputs I_0, I_1, I_2 & I_3 produced by inverted 2×4 Decoder are always set to logic 0 for the selected output and logic 1 for the other three outputs as shown in 2.2[10].

Transmission gates are most frequently utilized in circuits using XOR logic, such as complete adders and multiplexers, as the main switching portion. In any event, as demonstrated in, we consider the possibility of utility in line decoders when AND/OR logic is applied. Figure display the TGL AND/OR gates with two possible inputs. Even if they are completely swinging, not every combination of inputs produces a restoration. The two most prevalent types of circuits in pass-transistor logic are those that employ only NMOS pass transistors, such as CPL, as well as DPL and DVL, which use both PMOS and NMOS pass transistors. With this study, we focus on the DVL approach, in which full swing operation is preserved while DPL is improved fewer transistors. Figure display two input DVL AND/OR gates [11]. Similar to the TGL gates, They can swing but not restore. CMOS NAND/NOR gates require four transistors, but TGL/DVL gates only require three. presuming the presence of complementing inputs. High-fan-out circuits called decoders allow multiple gates to share a limited number of inverters. Using TGL/DVL gates facilitates transistor count reduction [12].

One significant similarity trait of these gates' asymmetry is one of their characteristics, are the reality that their input loads are not balanced. We identified the two The X and Y inputs to the gate are displayed in Figure 2.1 [2]. In TGL gates, input X controls the gate terminals of three transistors. while input Y is sent from the input to the output node through the transmission gate.

However, only one gate terminal is controlled by input Y in DVL gates, and it is routed to the output. The X and Y inputs of the gate will receive both the control signal and the propagation signal. This asymmetric characteristic allows a designer to arrange signals by deciding which input acts as the control and which one acts as the signal propagation of gate in each situation. When the propagating signal is a complimentary input, there is a considerable increase in latency since an inverter needs to be added to the propagation channel. It is greater effectiveness to use the Inverse variable as the control signal when using the inhibition (A'B) or implication (A'+B) function. The AND (AB) and OR (A+B) operations have the same power. Finally, regardless of whether you're working with A'+B' in NAND or A'B' in NOR any picking to make will unavoidably result in a complementing propagation signal [12].

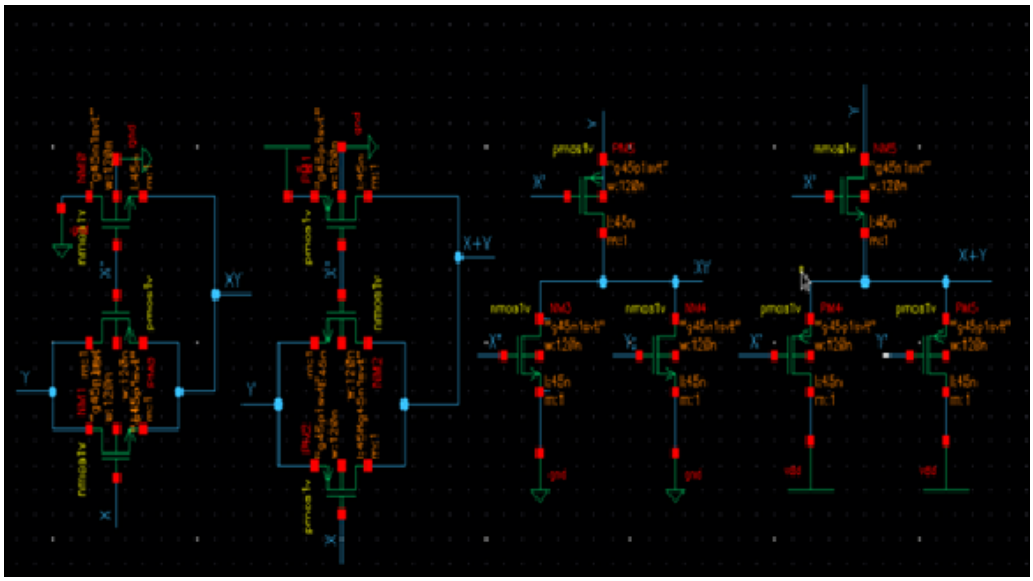

Fig. 2.1: (a) TGL AND gate , (b)TGL OR gate , (c) DVL AND gate ,(d) DVL OR gate

NAND and NOR gates have an advantage over AND and OR in typical CMOS architecture because they can express logic operations more efficiently with 4 transistors as compared to 6 transistors. It is possible to construct a 2×4 decoder using two inverters and four NOR gates. In contrast, an inverting decoder needs four NAND gates and two inverters which together produce "20" transistors.

Similarly the 16 min terms $D_0 D_{15}$ of the four input variables A, B, C, and D are produced by a Decoder with 4×16 lines, while the corresponding min terms $I_0 I_{15}$ are produced by inverted 4×16 line decoder. A predecoding approach, which divides blocks of n address bits into 1-of-2n pre decoded lines [12] that act as inputs to the final stage decoder, can be used to create such circuits. Pre decoding may be used to create such circuits [14]-[15]. As a result, two 2-four inverting decoders and sixteen 2-input NOR gates can be used to build a 4×16 decoder and two 2-four decoders and sixteen 2-input NAND gates can be used to implement an inverting one. These designs require eight inverters and twenty-four 2-input gates in CMOS logic, which adds up to "104" transistors per design [10].

2.1. 14T LP Topology for 2×4 Decoder (Non-Inverting). Developing a plan based on multiple logics A 2×4 decoder would require sixteen transistors altogether, two inverters, four TGL or DVL AND/OR gates, and two inverters. A 14 transistor decoder architecture is created by merging TGL and DVL AND gates in this design, which eliminates one of the two inverters, by carefully utilizing control and propagation signals.

In Figure 2.2 [1], the Decoder has two inputs A and B which produces the 4 min terms $D_0, D_1, D_2 \& D_3$,with the intention of removing inverter B. DVL AND gates are utilized to put into practice the min terms D_0 means (A'B') and D_2 means (AB'),where Signals A and B are transmitted .The TGL AND gate is employed to realize the min terms[12]. D_1 means (A'B) and D_3 means (AB), with B functioning as the propagate signal for D_1 means (A'B) and D_3 means (AB) each .The elimination of the B inverter is made possible by the choice of inputs and gates, resulting in a topology with 14T for the Decoder.

Figure2.3, demonstrates the simulation of 14T LP Topology 2×4 Decoder. When A=B=0,D_0 will enabled [14], when A=0 and B=1,D_1 will be enabled, when A=1 and B=0, D_2 will be enabled, when A=1 and B=1, D_3 will be enabled.

2.2. 14T LPI Topology for 2×4 Decoder (Inverting). Similarly, a 14T architecture with inverting 2 inputs 4 outputs Decoder can be built out of an inverter and four TGL/DVL OR gates.TGL /OR gates are utilized for min terms I_0 and I_2,while DVL OR gates are utilized to put into practice for min terms I_1 and I_3

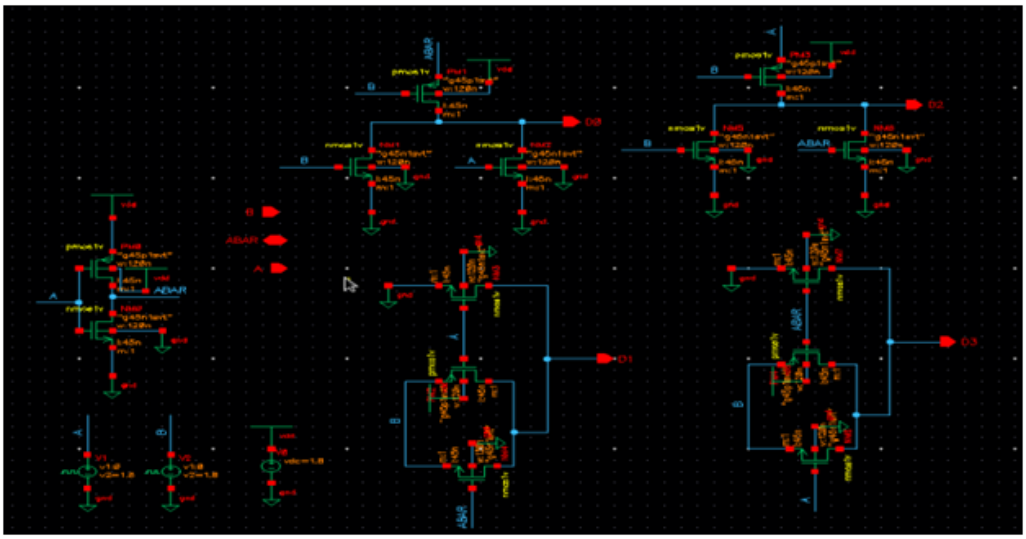

Fig. 2.2: 14T LP Topology for 2×4 Decoder (Non-Inverting)

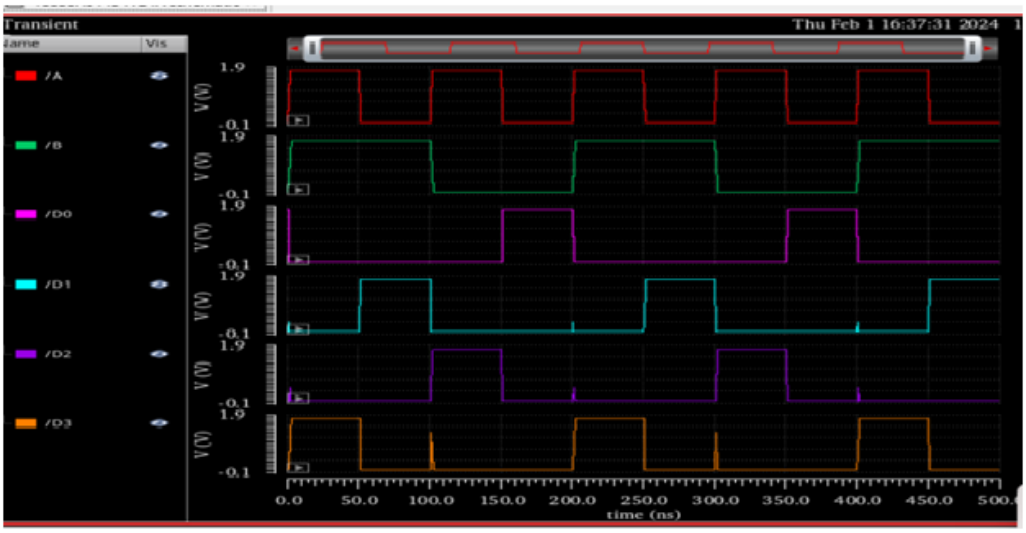

Fig. 2.3: Simulation result of 14T LP 2×4 Decoder (Non- Inverting)

are the output signal [16].The terms"2×4 LP" and "2×4 LPI," which "2×4 LP" stand for "Low power" and "2×4 LPI, stand for" Low Power Inverting" respectively, describe two LP Decoder architectures are used. These are shown Figure 2.2 and Figure 2.4.

Figure 2.5[1], demonstrates the simulation of 14T LPI Topology for 2×4 Decoder (Inverting). When A=B=0, I_0 will enabled, when A=0 and B=1, I_1 will be enabled, when A=1 and B=0, I_2 will be enabled, when A=1 and B=1, I_3 will be enabled.

2.3. 15T HP Topology for 2×4 Decoder (Non-Inverting). Due to the complimentary propagate signal utilized in minterms D_0 and I_3, One drawback of the above-discussed 14 transistor low power decoder topologies is their maximum latency. Due to their lack of requirement for complementary inputs, these minterms may be implemented using normal CMOS logic gates, which overcomes this disadvantage. minterm D_0 is

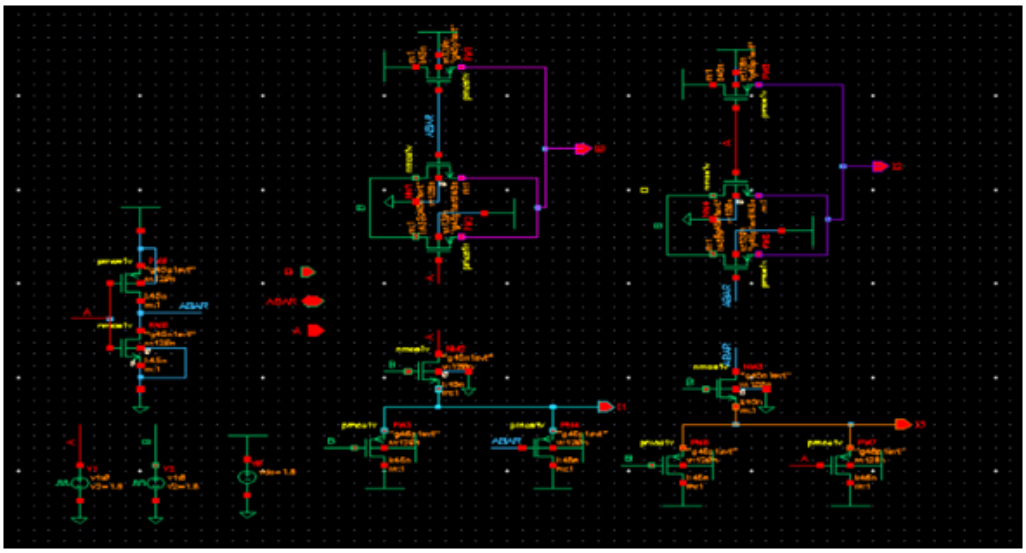

Fig. 2.4: 14T LPI Topology for 2×4 Decoder (Inverting)

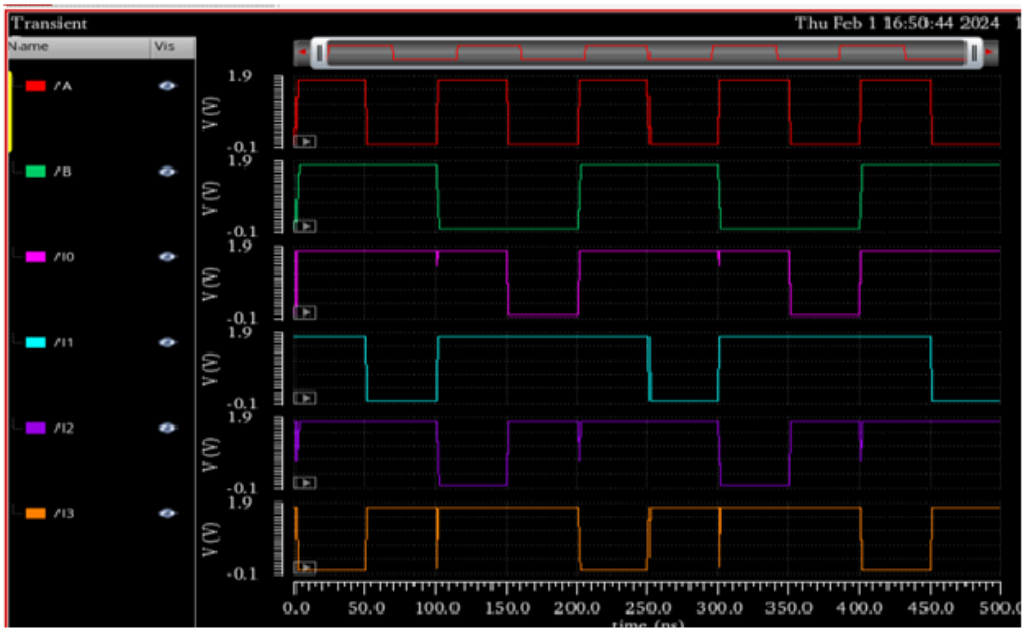

Fig. 2.5: Simulation result of 14T LPI 2×4 Decoder (Inverting)

put into practice using a CMOS NOR gate, while I_3 is constructed using a CMOS NAND gate. One more transistor is added to each structure. The resultant decoder structure, known as High Performance (HP) topology, comprises three distinct logic types in a single circuit(CMOS, TGL, and DVL) [17], improving power and delay performance are both excellent. The schematics of 2×4 HP decoder is as illustrated in Figure 2.6. This modification resulted in a Decoder architecture that has three distinct logic types in a single circuit(CMOS, TGL, and DVL) into a single circuit that improves power and timing efficiency. The HP topology describes

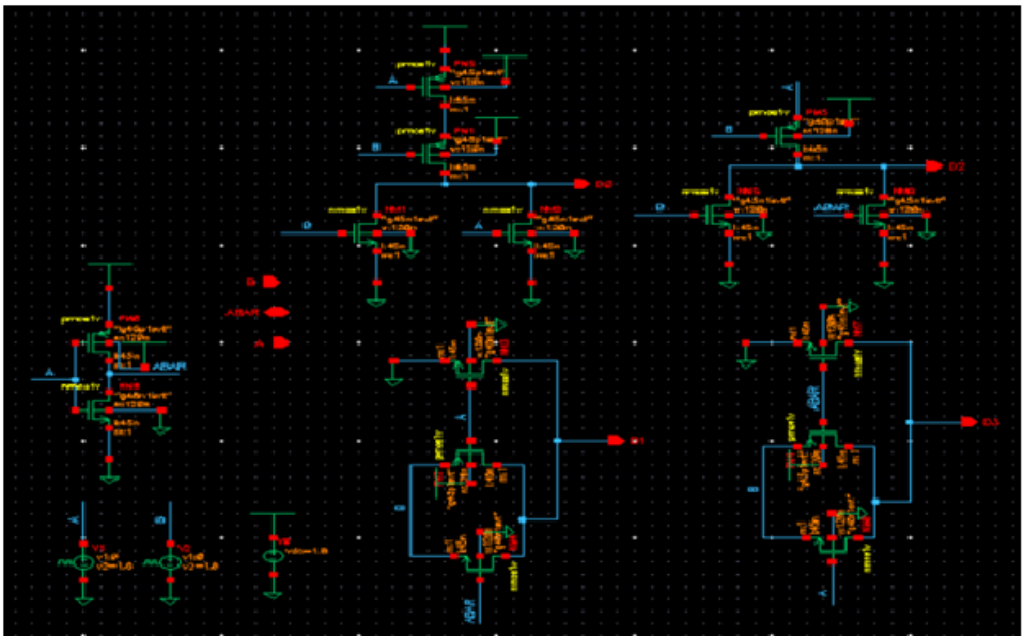

Fig. 2.6: 15T HP Topology for 2×4 Decoder (Non-Inverting)

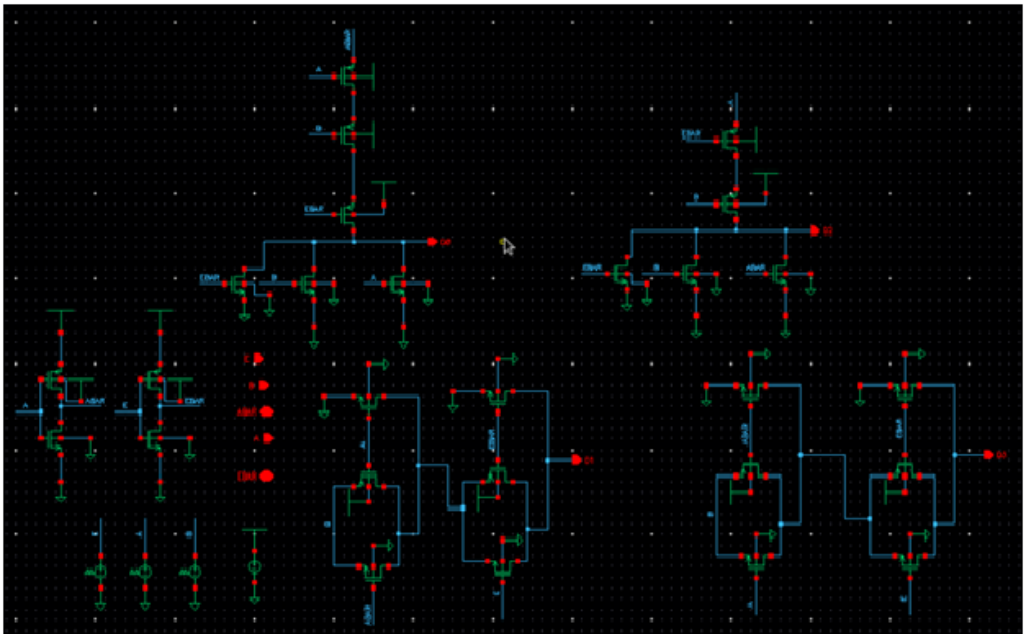

Fig. 2.7: Simulation result of 15T HP 2×4 Decoder (Non-Inverting)

this configuration specifically for its high throughput [9].

Figure 2.7[1], Shows the simulation of 15T HP Topology for 2×4 Decoder (Non-Inverting). When A=B=0, D_0 will enabled, when A=0 and B=1, D_1 will be enabled, when A=1 and B=0, D_2 will be enabled, when A=1 and B=1, D_3 will be enabled.

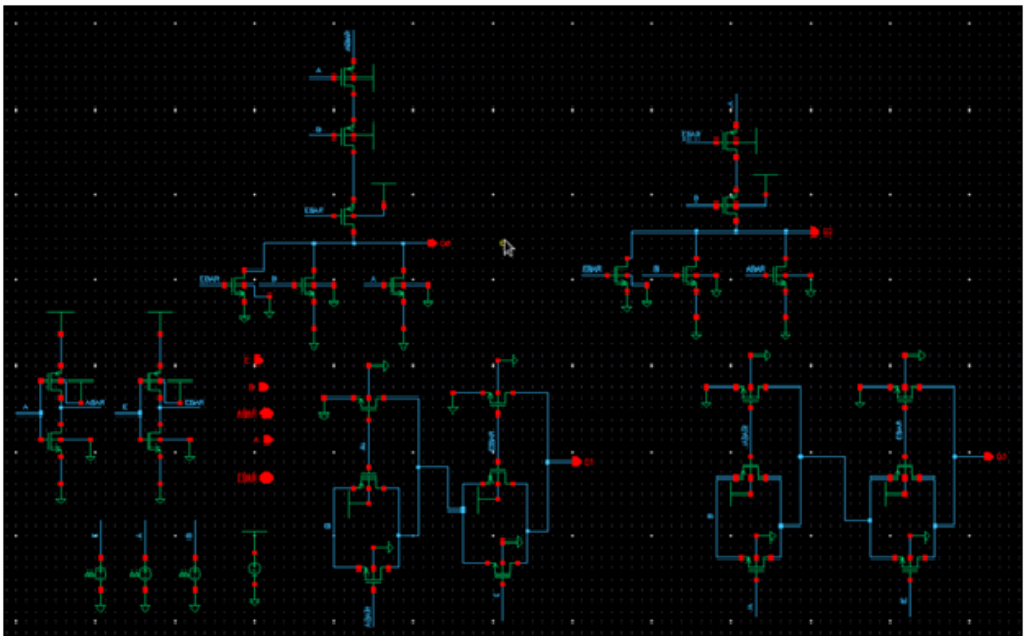

Fig. 2.8: 2×4 HP Mixed Logic Decoder with Enable (Non-Inverting)

2.4. 2×4 HP Mixed Logic Decoder with Enable (Non-Inverting). This section covers the design of decoders with enable input. The use of 2×4 decoder blocks can reduce the number of transistors in a n: 2n decoder. Since they don't need any extra logic gates, 2×4 decoders can be used to build higher stage decoders, which reduces design complexity. There are a number of benefits to logic gates are used in the post-decoder phases [18]– [22], including a reduction in wire delays and cross-talk caused by connections. However, the area overhead increases linearly with the number of logic gates needed. Only decoders without enable input are designed in every previous decoder study utilizing method of mixed logic design. This work uses the method of mixed logic design to construct decoders with enable input. The regulated functioning of decoder circuits is achieved with the addition of an enable input. In other words, only when the enable input is set to "on" does the decoder function, which also lowers dynamic power dissipation. Furthermore, instead of implementing at the transistor or gate level, it is always advised in contemporary techniques for chip design to construct macros or minor circuits that can be reused based on requirements.

A total of 30 transistors are needed for the non-reversing standard CMOS 2×4 decoder which includes enable, which also needs three NOR gates with three inputs and three inverters. DVL AND gates can be used to implement D_0 and D_2 in the 2×4 LP decoder which includes enable. A is used as the propagation signal, while EN and B are the signs of control; EN is the enable input. TGL AND gates are used to implement the minterms D_1 and D_3, with B serving as the propagation signal and A and EN serving as the signs of control.2×4 LP decoder which includes enable input requires 26 transistors. Similarly for 2×4HP decoder which includes enable input requires "27" transistors use a CMOS NOR gate with three inputs to replace D_0 minterm as shown In Figure 2.8

Figure2.8 [1], Shows the mixed logic line Decoder with enable. Inputs A and B produces $D_0, D_1, D_2 \& D_3$ as outputs. Figure 2.9, Shows the simulation of Mixed Logic 2×4 HP Decoder with Enable (Non- Inverting). When A=B=0, D_0 will be enabled, when A=0 and B=1,D_1 will be enabled, when A=1 and B=0, D_2 will be enabled, when A=1 and B=1, D_3 will be enabled.

3. Proposed Methodology. A novel 2×4 Decoder with only 12T Transistor is proposed with area optimization in this research. CMOS logic is additionally used for execution of 2×4 Decoder. Delay and power is used for evaluation between the novel design and CMOS logic. The novel design of 2×4 Decoder [1] is Less

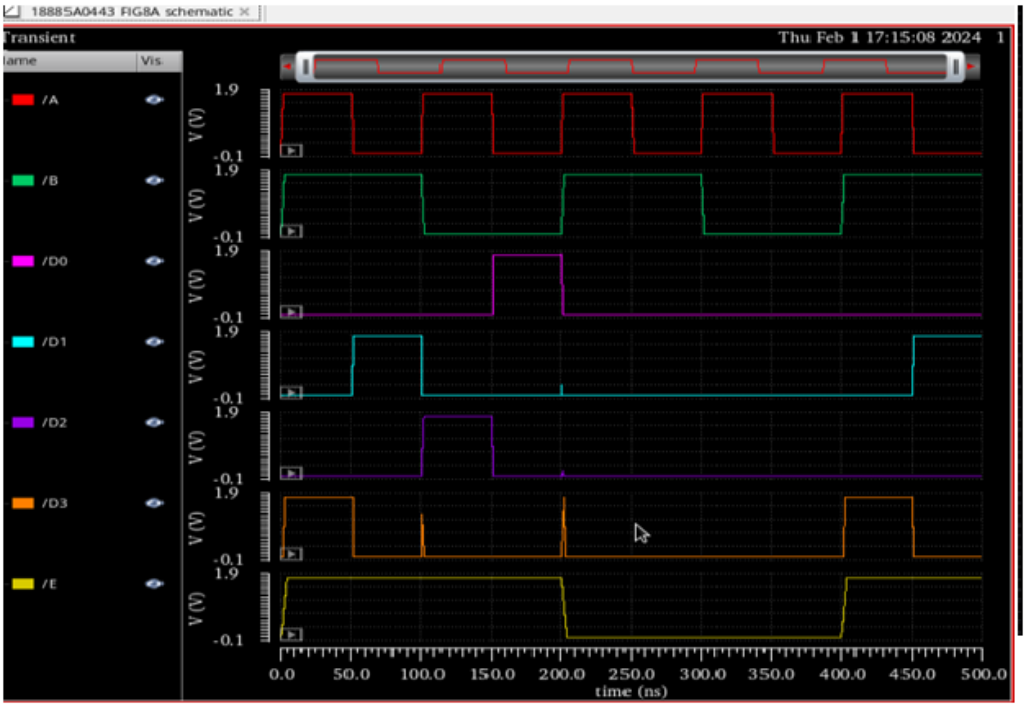

Fig. 2.9: Simulation of New Mixed-Logic 2×4 HP Decoder with Enable (Non-Inverting)

Table 3.1: Truth table for 2×4 LP Decoder

A	**B**	D_1	D_2	D_3	D_4
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

optimized for power in contrast to CMOS logic design at a typical value of 1.8V.

The LP circuit designs is a requesting issue in high performance digital frameworks, for example, microchips, DSPs and other different applications. Power and speed are the main high lights considered while comparing any circuit or design. Diminishing chip area is additionally truly impressive factor, creators need to recall when suggesting any novel design. Decoder is used for conversion of binary inputs to associated output bits in a pattern. There are wide range of applications of Decoder such as seven-segment display, data de-multiplexing, etc. Numerous studies using sequential and combinational circuits are currently being conducted different logics.

3.1. 12T LP Topology for 2×4 Decoder (Non-Inverting). Decoders are crucial circuits, for the most part utilized in the hardware involving collections of RAM [19]. In this study, we propose an innovative approach to putting them into practice, which rapidly decreases the amount of transistors in 2×4 Decoder circuit. Power and area efficient Decoders with less number of transistors plays a very significant role in circuit designing and act as elementary units. Figure 3.1 Shows proposed non inverting 2×4 Decoder generates 4 min terms $D_1, D_2, D_3 \& D_4$ with two inputs A and B and its truth table is shown in below Table 3.1.

The proposed circuit for implementation of 12T LP 2×4 Decoder designed using CMOS and Dual Value Technique is shown in Figure 3.6. One of the four outputs is choosen and set to 1 depending on the input

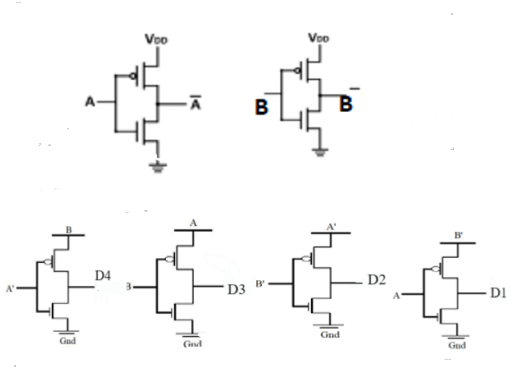

Fig. 3.1: Proposed 2×4 Decoder with 12T

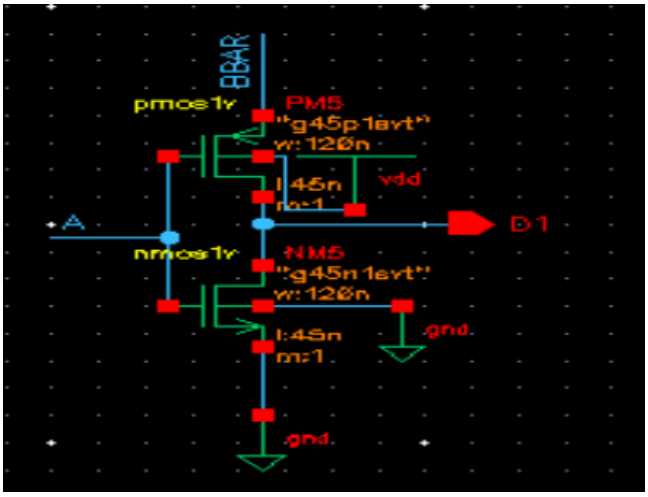

Fig. 3.2: 12T LP Topology for 2×4 Decoder with "D_1" data output

combination, while the other three are set to 0 [7].

3.1.1. 12T LP Topology for 2×4 Decoder with " D_1" data output. The proposed circuit for implementation of 12T LP 2×4 Decoder designed using CMOS and Dual Value Technique is shown in Figure 3.6. First term "D_1" using proposed design as shown in Figure 3.2 is both PMOS and NMOS gates has been connected with input A, PMOS drain has connected with one of the input complement of B. "D_1". will be formed by the combination of the PMOS and NMOS linked to the output

3.1.2. 12T LP Topology for 2×4 Decoder with "D_2" data output. The proposed circuit for implementation of 12T LP 2×4 Decoder designed using CMOS and Dual Value Technique is shown in Figure 3.6. Second term "D_2" using proposed design as shown in Figure 3.3 is both PMOS and NMOS gates has been connected with input complement of B, PMOS drain has connected with one of the input complement of A. PMOS and NMOS combined with their connections to the output will result in a "D_2".

3.1.3. 12T LP Topology for 2×4 Decoder with "D_3" data output. The proposed circuit for implementation of 12T LP 2×4 Decoder designed using CMOS and Dual Value Technique is shown in Figure 3.6. Third term "D_3" using proposed design as shown in Figure 3.4 is both PMOS and NMOS gates has been connected with input B, PMOS drain has connected with one of the input A. A "D_3" will be produced by connecting PMOS and NMOS.

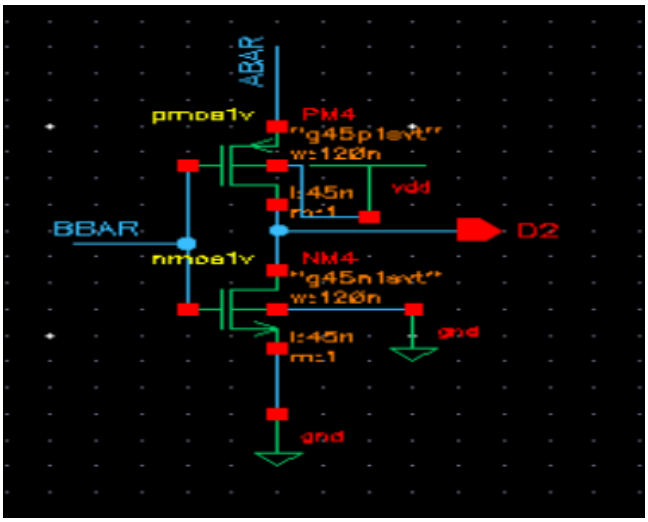

Fig. 3.3: 12T LP Topology for 2×4 Decoder with "D_2" data output

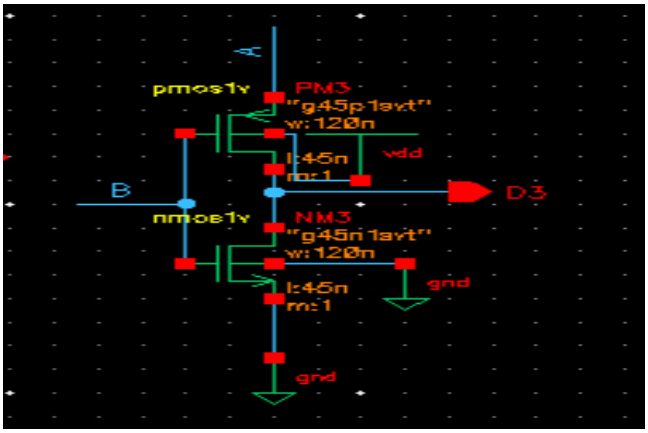

Fig. 3.4: 12T LP Topology for 2×4 Decoder with"D_3" data output

3.1.4. 12T LP Topology for 2×4 Decoder with "D_4"data output. The proposed circuit for implementation of 2×4 Decoder designed using CMOS and Dual Value Technique is shown in Figure 3.6. Fourth term "D_4" using proposed design as shown in Figure 3.5 is both PMOS and NMOS gates has been connected with input complement of A, PMOS drain has connected with one of the input B. The combination of the both PMOS and NMOS linked to the output will produce data
" D_4".

The proposed circuit 12T LP Topology for 2×4 Decoder has been validated with Cadence Virtuoso with 45GPDK Technology. The entire technology designed with CMOS and Dual Value Methodology shown in Figure 3.6.

Figure 3.7 Shows the simulation of Non-Inverting 12T LP Topology for 2×4 Decoder with CMOS and DVL topology. When A=B=0, D_1 will enabled, when A=0 and B=1, D_2 will be enabled, when A=1 and B=0, D_3 will be enabled, when A=1 and B=1, D_4 will be enabled.

3.2. 12T LPI Topology for 2×4 Decoder (Inverting). Figure 3.8 shows 12T 2×4 Decoder in inversion mode. It contains two inverters that will produce complement of A and complement of B. i.e A' and B'. A 2×4

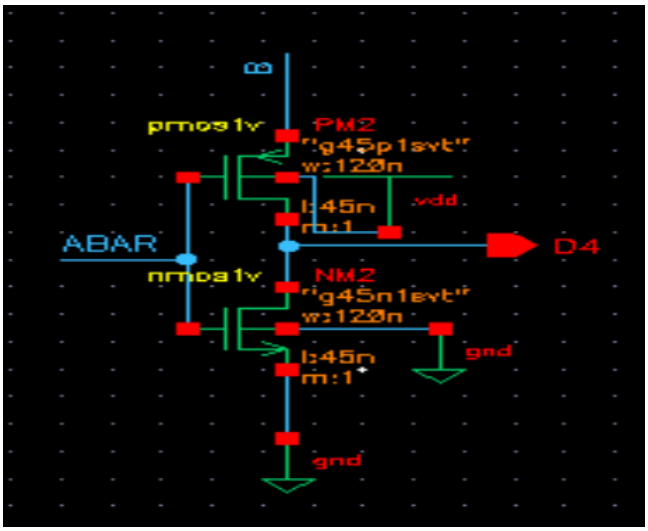

Fig. 3.5: 12T LP Topology for 2×4 Decoder with "D_4" data output

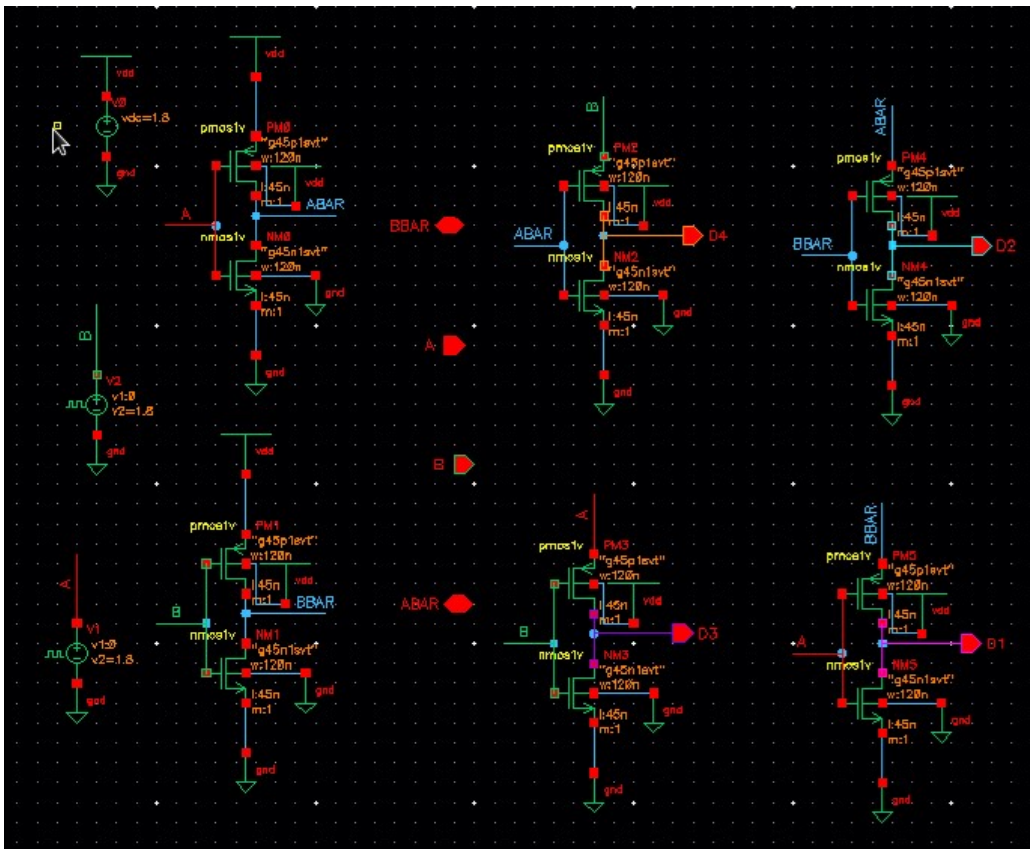

Fig. 3.6: Non-Inverting 12T LP Topology for 2×4 Decoder

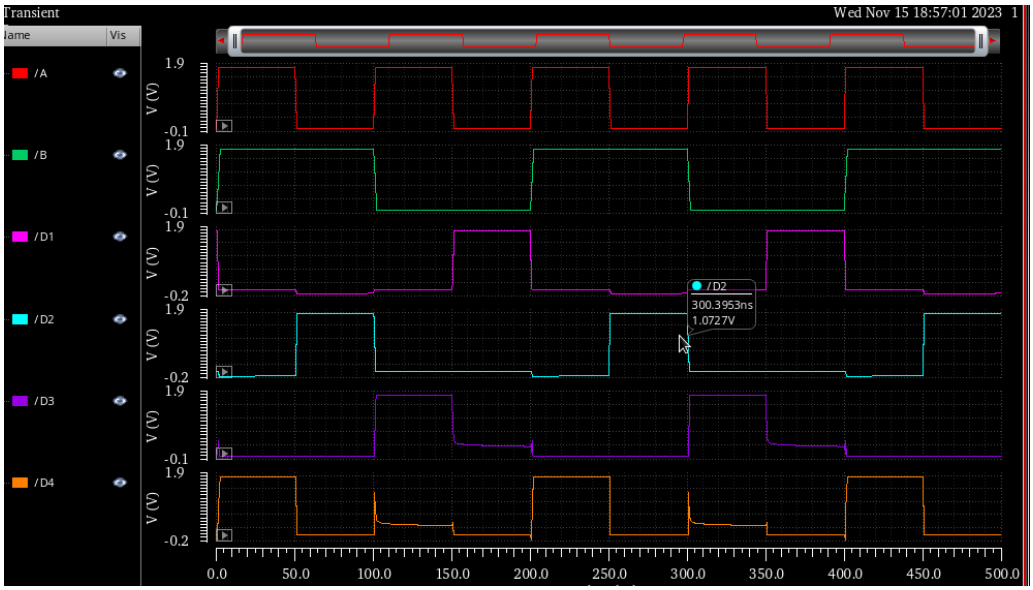

Fig. 3.7: Simulation result of Non-Inverting 12T LP 2×4 Decoder

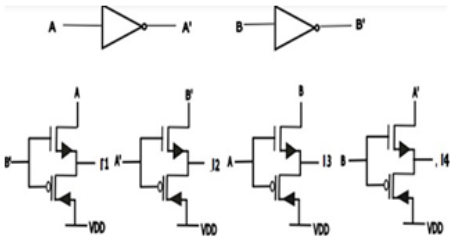

Fig. 3.8: 12T LPI Topology for 2×4 Decoder (Inverting)

Table 3.2: Truth table for 2×4 LPI Decoder (Inverting)

A	**B**	I_1	I_2	I_3	I_4
0	0	0	1	1	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	1	1	1	0

LPI Decoder generates the 4 minterms $I_1, I_2, I_3 \& I_4$ of two inputs A and B and its truth table is shown in Table 3.2.

3.2.1. 12T LPI Topology for 2×4 Decoder (Inverting) with "I_1" data output. The proposed circuit for implementation of 12T LPI 2×4 Decoder designed using CMOS and Dual Value Technique as shown in Figure 3.13. First term "I_1" using proposed design as shown in Figure 3.9 is both PMOS and NMOS gates has been connected with complement of B, NMOS drain has connected with one of the input A. PMOS source is connect with V_{DD}. The combination of the both PMOS and NMOS connected to the output will produce

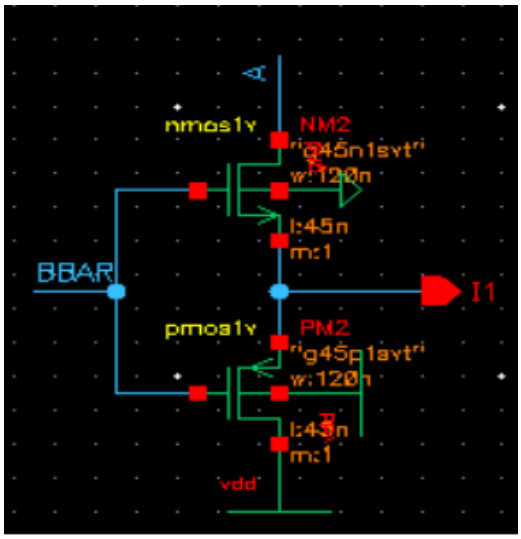

Fig. 3.9: 12T LPI Topology for 2×4 Decoder (Inverting) with "I_1" data output.

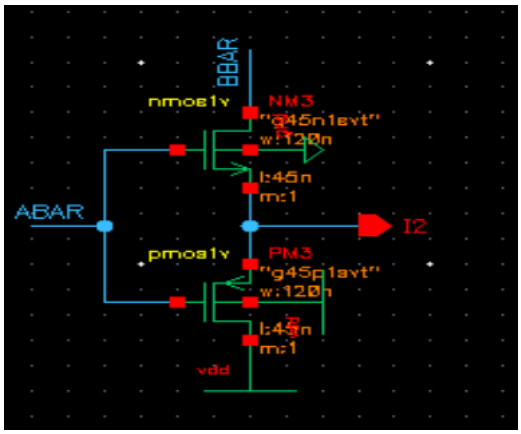

Fig. 3.10: 12T LPI Topology for 2×4 Decoder (Inverting) with "I_2" data output.

data "I_1".

3.2.2. 12T LPI Topology for 2×4 Decoder (Inverting) with "I_2" data output. The proposed circuit for implementation of 12T LPI 2×4 Decoder designed using CMOS and Dual Value Technique as shown in Figure 3.13. Second term "I_2" using proposed design as shown in Figure 3.10 is both PMOS and NMOS gates has been connected with complement of A, NMOS drain has connected with one of the input complement of B. PMOS source is connect with V_{DD}. The combination of the both PMOS and NMOS connected to the output will produce data "I_2".

3.2.3. 12T LPI Topology for 2×4 Decoder (Inverting) with "I_3" data output. The proposed circuit for implementation of 12T LPI 2×4 Decoder designed using CMOS and Dual Value Technique as shown in Figure 3.13. Third term "I_3" using proposed design as shown in Figure 3.11 is both PMOS and NMOS gates has been connected with input A, NMOS drain has connected with one of the input B. PMOS source is connect with V_{DD}. The combination of the both PMOS and NMOS linked to the output will produce data "I_3".

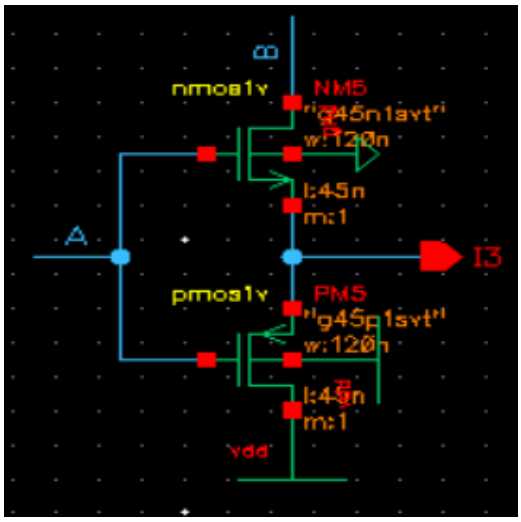

Fig. 3.11: 12T LPI Topology for 2×4 Decoder (Inverting) with "I_3" data output.

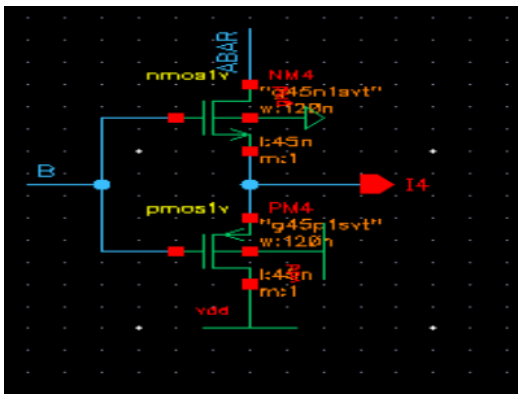

Fig. 3.12: 12T LPI Topology for 2×4 Decoder (Inverting) with "I_4" data output.

3.2.4. 12T LPI Topology for 2×4 Decoder (Inverting) with "I_4" data output. The proposed circuit for implementation of 12T LPI 2×4 Decoder designed using CMOS and Dual Value Technique as shown in Figure 3.13. Fourth term "I_4" using proposed design as shown in Figure 3.12 is both PMOS and NMOS gates has been connected with input B, NMOS drain has connected with one of the input complement of A. PMOS source is connect with V_{DD}. The combination of the both PMOS and NMOS connected to the output will produce data "I_4".

The proposed circuit 12T LPI Topology for 2×4 Decoder has been validated with Cadence Virtuoso with 45GPDK Technology. The entire technology Designed with CMOS and Dual Value Methodology as shown in Figure 3.13.

Figure 3.14, Shows the simulation results of 12T LPI Topology for 2×4 Decoder with CMOS and DVL Topology. When A=B=0, I_1will enabled, when A=0 and B=1, I_2 will be enabled, when A=1 and B=0, I_3 will be enabled, when A=1 and B=1, I_4 will be enabled.

4. Results and Discussion. Every simulation is run using the 45 GDPK technology Cadence Virtuoso tool. The Table 4.1 shows that when comparison with the proposed 12T 2×4 LP LP and LPI Decoders, with existing 2×4 LP Decoders, Since the suggested approaches increase power with a delay overhead and fewer

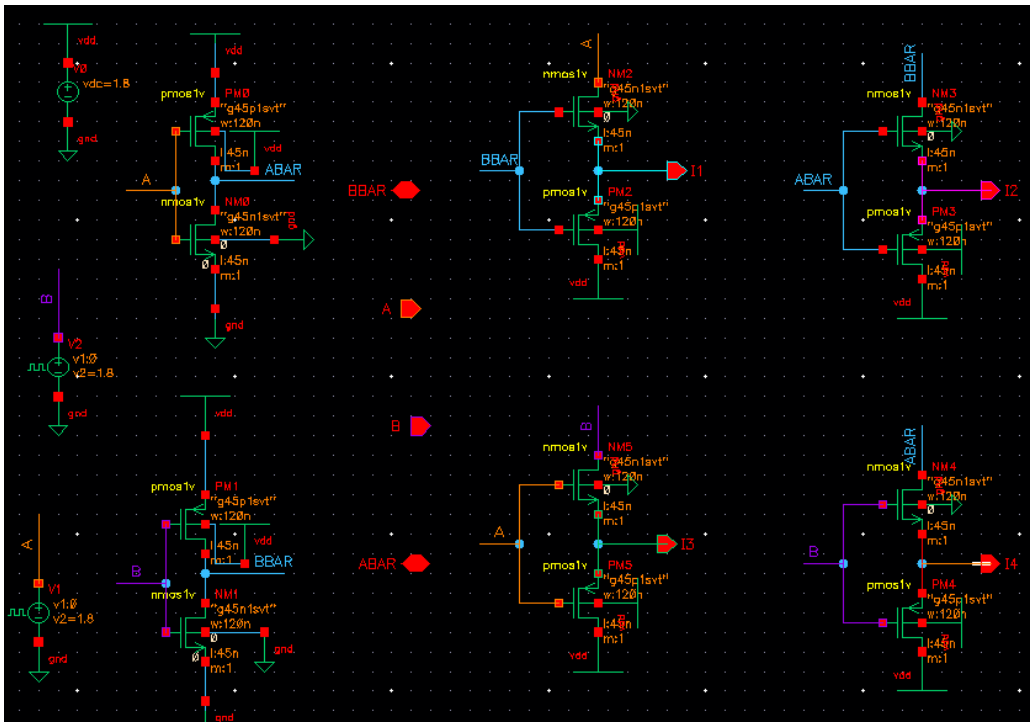

Fig. 3.13: Inverting 12T LPI Topology for 2×4 Decoder

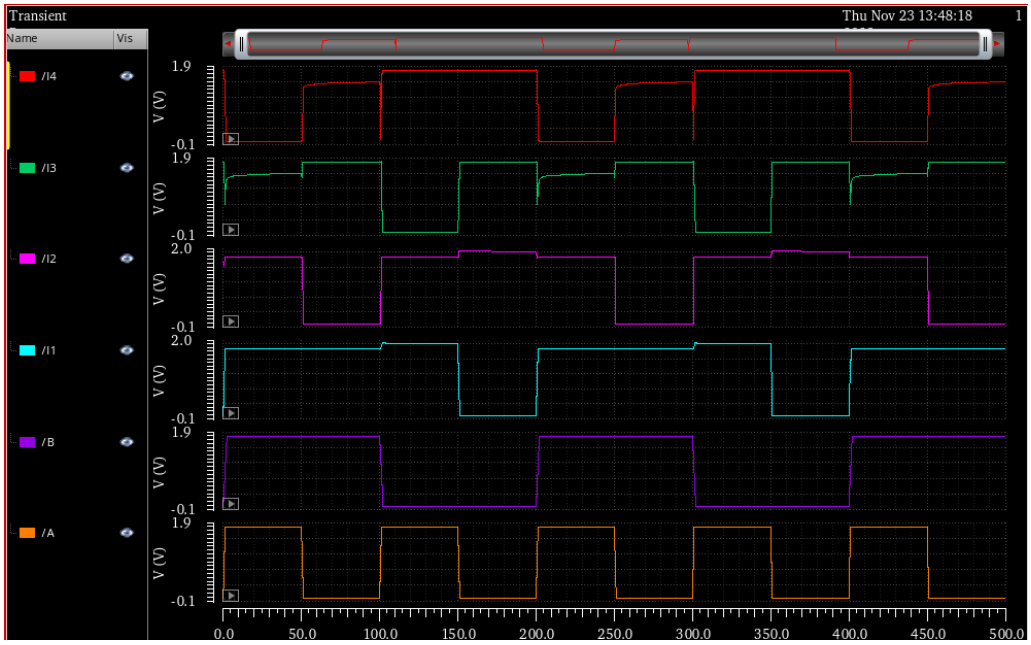

Fig. 3.14: Simulation result of Inverting 12T LPI 2×4 Decoder

Table 4.1: Comparison of Results

S.No	Method Decoder	AVG Power (w)	Static Power (w)	Dynamic Power (w)	Delay (sec)
1	14T LP	509.8E-9	721 p	80.69 μ	100.7E-9
2	14T LPI	530.8E-9	680.47 p	992.41 p	211.8E-12
3	15T HP	572.5E-9	730.5 p	87.143 μ	50.23E-9
4	15T HPI	16.81E-6	680.04 p	54.15 μ	210.6E-12
5	26T LP	726.8E-9	1.07 n	82.97 μ	149.5E-9
6	26T LPI	32.82E-3	1.39 n	66.44 μ	100.3E-9
7	26T HP	724.0E-9	1.12 n	83.91 μ	150.3E-9
8	26T HPI	32.82E-3	1.474n	66.44 μ	100.9E-9
9	12T LP Proposed	1.129E-6	105.28 p	5.36 μ	631.2E-12
10	12T LPI Proposed	651.9E-9	1.053 n	37.51 μ	50.34E-9

transistors, they are suitable for scenarios where size and power loss are the main design issues. The two innovative topologies (CMOS and DVL) used in the design of the proposed decoders are low power and low power inverting, respectively. The propagation delay, the circuit's static and dynamic powers, and the overall average power are computed in each scenario. For simulation, an operating voltage of 1.8V is utilized. When compared to their typical CMOS predecessors, All of the Applied decoders can swing freely and have fewer transistors. The suggested 12T 2×4 LP decoder consumes average power of 1.129 µw, static power of 105.28 pw, dynamic power of 5.36 µw and delay of 631.2 ps and 12T 2×4 LPI decoder consumes average power of 651.9 nw, static power of 1.053 nw, dynamic power of 37.51 µw and delay of 50.34 ns. The results for 12T LP 2×4 and 12T LPI 2×4 Decoders are tabulated in Table 4.1

5. Conclusion. The design in this research was validated using Cadence Virtuoso 45GPDK Technology. An efficient Decoders deigned by blending DVL Topology with static CMOS. Simulation results prove that, when comparison with the proposed 12T LP, LPI Decoders with existing 2×4 LP, LPI Decoders provides the upgrade in power with an upward on delay with diminished quantity of transistors and are acceptable for operations in area and power dissipation are the crucial device consideration. The 2×4 Decoders implemented has essentially less number of transistors so it will inhabit less on chip area as compared to CMOS logic which can be observed from 4.1. The novel design is 60.72% optimized for power as compared to CMOS Logic design at a typical value of 1.8V which can also be observed from the Table 4.1. these Implemented Decoders have full swing capacity and diminished quantity of transistors count in contrast to usual CMOS counterparts.

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